ANALYSIS OF PERFORMANCES FOR STATIC POWER-CONDITIONING SYSTEMS - INVERSION, CONVERSION, AND REGULATION

Prepared by

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ABSTRACT
(Electrical Engineering)

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ABSTRACT

In the past decade, the new needs of the space programs have furnished a powerful impetus to the sudden and widespread activity in the developments of direct energy conversions such as from heat or light into electricity. Thus far, these sources have been characterized by the low dc voltage outputs that vary with the environmental conditions such as temperature or light intensity. However, the spacecraft electrical loads normally require power at various forms and voltage levels that are quite different from the low dc outputs of these sources. As a consequence, certain power-conditioning systems are required to provide the necessary compatibility between these unconventional sources and the spacecraft loads.

Three of the more important functions performed by these power-conditioning systems are (1) the step-up of low source voltages, (2) dc to dc conversion with regulation, and (3) dc to sinusoidal ac inversion with regulation at specified frequencies. In the research that leads to the writing of this dissertation, attention has been given to each of these three functional areas, with each area being represented by a specific

system which performs one of the three aforementioned functions. This work consists of the analytical and experimental investigations of the following three systems:

(1) The Marzolf tunnel diode inverter for voltage step-up.

(2) An efficient and physically simple dc to dc regulated converter using the basic principle of inductive-energy storage.

(3) A light-weight, self-regulating dc to sine-wave inverter utilizing techniques of high-frequency pulse-width modulation.

In addition to the new circuit developments, several important analytical results are obtained from these studies. With respect to each of the three systems, the more important results include:

(1A) The understanding of the significance of the source inductance as a circuit element in the Marzolf inverter, its effect and its relationship with the zero-voltage step interval associated with the induced-voltage waveform of the inverter.

(1B) The calculations of the voltage spikes at the leading edges and the voltage curvatures at the trailing edges of the inverter induced-voltage waveform.

(2A) An analytical comparison of frequency ranges among different types of variable-frequency dc to dc regulated converters using the principle of inductive-energy storage in their inverter stages.

(2B) An understanding of the ringing phenomenon exhibited by converters using the principle of inductive-energy storage during light-load conditions.

(3) The analytical proof of negligible harmonic amplitudes which provides the mathematical foundation of the pulse-width modulation technique as applied to dc to sinusoidal ac inversion.

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My appreciation also goes to Mr. Robert L. Penley for his general laboratory help in his customarily superb manner. In connection with this dissertation, it is through his talented hands that all the test circuits are wired and many of the illustrations are traced.

I would be remiss if I did not acknowledge the influence of Dr. Edward T. Moore in the development of my research program, particularly at its early stage.

Most important among those to whom acknowledgments are due for help in one or another of the stages through which this work has passed in evolution and preparation is Dr. Thomas G. Wilson, the Principal Investigator of this NASA project. Without his guidance and encouragement, my research would not have progressed to the present stage. As my teacher in electrical engineering and quite often in English and others as well, Dr. Wilson has unwittingly inspired and influenced me in numerous ways since I became a foreign student at Duke University five years ago. He is not only a great teacher to whom I have great respect and admiration, he is also, and I hope he would tolerate my lack of elegance here, my "big uncle away from home."

Finally, it would not be adequate to give formal thanks to my mother, Mrs. Fay Yu, who could not live to see this acknowledgment, to my father, Dr. Yao-nan Yu, and to my wife Grace Hu Yu. Their love, patience, inspiration, and understanding have made this work their accomplishment as well as mine.

Yuan Yu

CONTENTS

CONTENTS (continued)

LIST OF FIGURES

LIST OF FIGURES (continued)

LIST OF FIGURES (continued)

ANALYSIS OF PERFORMANCES FOR STATIC POWER-CONDITIONING SYSTEMS - INVERSION, CONVERSION, AND REGULATION

CHAPTER I

INTRODUCTION

In the past decade unconventional power sources such as fuel cells, solar cells, thermoelectric and thermionic converters, have been developed to a stage that their power capabilities are ample for practical space applications.[1] However, all these devices are characterized by their low-voltage high-current outputs. Due to the requirements of spacecraft electrical loads for power at certain higher dc voltages or for power in the form of alternating current at specified frequencies, the direct utilization of power from these unconventional sources with very low dc output voltages often is not possible. One solution to the problem of producing higher dc voltages would be to connect many individual sources in series in order to achieve more practical voltage levels. Another solution would be to employ certain voltage-transforming and step-up systems to achieve the desired output levels. Each of these two approaches has its own merits. In general, the former approach results in the more efficient utilization of the source power, while the latter one is often more reliable especially when the output voltage is high. Regardless of the approach used, the

available voltage levels are functions of environmental conditions of the sources such as temperature and light intensity. However, most of the spacecraft electrical loads require dc or ac voltages that are closely regulated. In order to achieve the necessary compatibility between these sources and various electrical loads, certain power-conditioning processes are required to accomplish the desired electrical to electrical transformations.

Reliability is important due to the lack of maintenance of the spacecraft electrical systems, while a higher efficiency means less input power for a certain output load which, in turn, reduces the power capacity required of the source as well as its weight. Reliability, weight, and efficiency are therefore three of the major concerns in designing any spacecraft power-conditioning system. Normally, these aspects impose conflicting design requirements, and may be traded one for the other. Consequently, either proper compromises must be made to achieve the best overall performance or special attention be given to one particular aspect at the expense of the others. In connection with these different emphases there have been numerous publications in the past decade concerning these three aspects of spacecraft power-conditioning systems.

Depending on the input conditions and output requirements, three of the more important functions performed by these power-conditioning systems which operate between the sources and the loads are: (1) the step-up of direct voltage from a source with output of a fraction of a volt to higher levels required by the output loads, (2) the change of an input voltage in the range

of tens of volts (obtained from series connection of low-voltage sources) which may fluctuate with the changing environmental conditions or the variable load demands to a regulated output dc voltage whose amplitude is essentially constant, and (3) the transformation of a variable dc voltage in the range of tens of volts to a regulated sinusoidal output voltage whose frequency and amplitude are essentially constant. During the period of research that leads to the writing of this dissertation, attentions have been given to all these three different areas. Selective topics in each of these areas of power-conditioning systems are reported in the following three chapters, with emphases on the understanding of the system operations and their potential applications.

Chapter II deals with the step-up of voltage from a low-voltage source to higher acceptable levels for electrical loads mentioned as area (1). The inherent low-voltage electrical characteristic of the tunnel diode makes it one of the most practical devices suitable for this type of application.[2] One of the tunnel diode circuits which perform the voltage step-up with inherent reliability is the Marzolf inverter consisting of two tunnel diodes and one square-loop core.[3] Because of its physical simplicity and its rather sophisticated switching phenomenon, this inverter is chosen as the topic for an analytical study. Since its introduction, much energy and talent by many people have been directed toward the understanding of this circuit. Some studies have been concentrated on its performance characteristics such as efficiency and voltage regulation, thus,

neglecting the finer details of its complex switching phenomenon. Other investigation has been purely mathematical analysis in which a single nonlinear differential equation is used to describe the overall inverter operation, thus giving an over-simplified picture and leading to some incorrect conclusions. The steady-state performances of this inverter are analyzed in Chapter II by using a combined graphical and analytical technique. Special attentions are given to the natures and the calculations of many functional subtleties of the inverter which have been experimentally observed, yet without satisfactory physical explanations or mathematical analyses. One of the important new findings in Chapter II is the effect of source inductance. It is found that the inadvertent existences of small amount of inductances in the sources and the transmission lines supplying power to the inverters often are primarily responsible for the tunnel diode switching patterns reported previously in the literature. The other important result is the calculation of the entire induced-voltage waveform including the amplitudes of the voltage spikes at the beginning of each half cycle. By extending similar techniques to the analyses of other types of magnetically-coupled multivibrators such as the Royer circuit,[4] it is hoped that the switching phenomena of such more complexed inverters can be thoroughly understood.

Although the Marzolf inverter analyzed in Chapter II provides a simple and reliable means for voltage step-up, the efficiency of the inverter is quite low due to the inherent nonlinear i-v characteristics of tunnel diodes. For better inversion efficiency, other semiconductors such as transistors

and controlled rectifiers are operated as switches in other magnetically-coupled multivibrators such as the Royer circuit and the series inverter circuit. In order to be able to utilize efficiently the higher voltage ratings of these devices, dc input voltages to the transistor or SCR inverters are normally much higher than those to the tunnel diode inverters. The higher voltages are obtained from the series connections of many low-voltage sources. Due to the changing environmental conditions of the sources and the varying demands of the loads, the output voltage of each low-voltage dc source, and therefore the sum of the series-connected voltages, are not constant. However, regulated dc voltages are often desirable for space applications due to the constant voltages demanded by different electrical loads of the spacecraft and various experiments being conducted aboard the spacecraft. Regulated dc to dc converters mentioned earlier as area (2) therefore become a part of particular importance to the spacecraft power-conditioning systems. Primarily because of its potentially high efficiency and its physical simplicity, a nondissipatively-regulated dc to dc converter using the basic principle of inductive-energy storage was designed and is described in Chapter III. Regulation of the converter is accomplished by controlling both the on time and the off time of its main power transistor. The frequency range over which the inverter stage of this converter operates is smaller than that of the other variable-frequency converters. This smaller frequency range causes less difficulty in making the proper compromises among the various performance

characteristics involving weight, efficiency, output ripple, transient response, and system stability, thereby contributing materially to the good overall performance of this converter. Converter operation under different line and load conditions is analyzed in detail in Chapter III.

In certain space applications dc to ac inverters are required to supply low-frequency sinusoidal voltages to the output loads mentioned earlier as area (3). A major concern in designing such dc to sine-wave inverters has been the weight and size of the output transformers and the output filter components as they have often been dictated by the low frequency of the sinusoidal output voltage. Through the use of digital techniques and unique transformer connections, an unfiltered output voltage having small total harmonic distortion has been reported in the literature.[5,6] The low harmonic contents have resulted in size and weight savings in the output filter, yet they still require a transformer to process the output power of the inverter at the desired low frequency. More recent developments in the dc to sine-wave inverter have involved the pulse-width modulation technique in which the requirements for both the output transformer and the low-frequency filter components are eliminated.[7] Here, the desired low-frequency sinusoidal output is extracted from a repeating pattern of alternating high-frequency square pulses all having equal amplitudes. The widths of successive pulses in the pattern are controlled to vary sinusoidally in accordance with a reference sinusoidal signal of the desired low frequency. While the small

harmonic amplitudes produced by this technique has been asserted intuitively and demonstrated experimentally, there has been no rigorous mathematical proof to support this fact. Chapter IV presents the circuit and the analysis of a newly-developed physically-simple dc to sine-wave inverter using this technique. Small amplitudes of the harmonics of the fundamental sinusoidal output voltage that are observed experimentally is also proved analytically, thus providing a mathematical foundation for the technique of pulse-width modulation. The analysis also proves the experimentally-confirmed self-regulating property of this inverter, thus increasing its versatility and its potential for practical applications.

As a summary, this dissertation consists of the analytical and experimental studies of three systems, one in each of the three more important areas of spacecraft power conditioning. They are the voltage step-up from extremely low voltage sources, the dc to dc conversion with regulation, and the dc to sinusoidal ac inversion. Through the new theoretical findings and the new practical developments, it is hoped that this study may contribute to the better understandings and to the advancements of the state of art in the field of spacecraft power-conditioning systems.

CHAPTER II

ANALYSIS OF THE MARZOLF TUNNEL DIODE INVERTER

In the past few years, the new needs of the space program have caused widespread development of direct energy conversion such as from heat or light into electricity. However, many of these sources are characterized by a low dc output voltage which is not readily applicable to various types of electrical loads aboard the spacecraft. There are many ways to raise this voltage to a higher level, one of which is to employ an inverter to change the low dc voltage into an ac square wave and transform it into higher voltage level. The Marzolf tunnel diode inverter, consisting of two tunnel diodes and one square-loop core, is one of the many circuits which can accomplish this voltage transformation with physical simplicity and inherent reliability.[3]

Two representative square-wave induced-voltage waveforms of the Marzolf inverter are shown in Fig. 2.1. In Fig. 2.1(A) which corresponds to the conditions most normally encountered in this inverter, a constant-voltage plateau from point u to w is seen to exist between a voltage spike from a to u and a voltage curvature from w to b. In Fig. 2.1(B) which

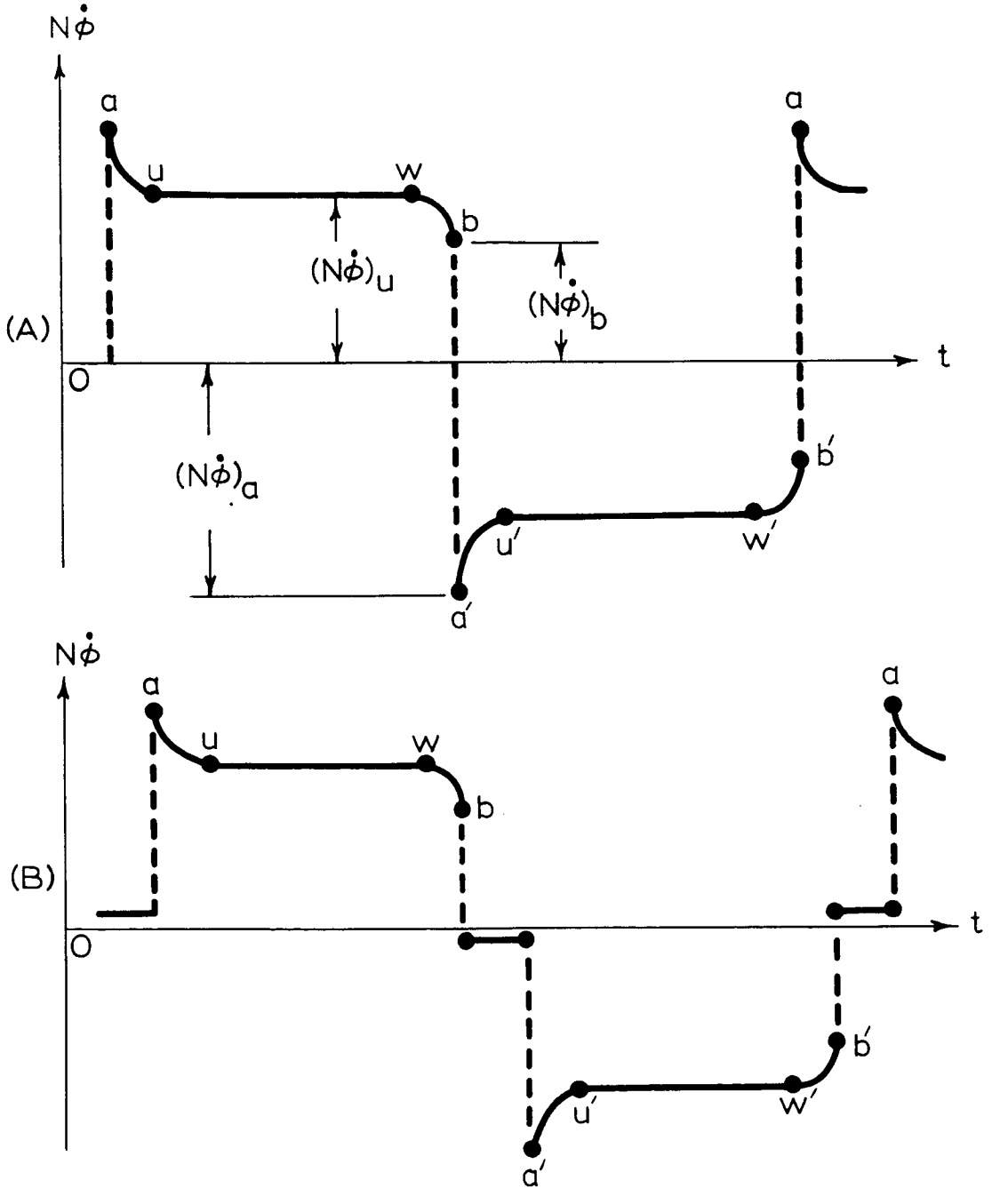


Fig. 2.1. Induced-Voltage Waveform of Marzolf Inverter.

(A) Without Small-Voltage Steps
(B) With Small-Voltage Steps

corresponds to conditions often encountered in Marzolf inverters using tunnel diodes of high current ratings, an additional time interval of almost zero voltage is seen to exist between the positive and negative voltage levels, resembling a delay at the beginning of every half cycle of the otherwise-normal square-wave output.[8,9]

The understanding of the nature of the voltage spikes and of the voltage curvatures are of considerable importance since they determine the quality of the square-wave output. It is generally known that the amplitudes of the voltage spikes and of the voltage curvatures, i.e., $\left[(N\dot{\phi})_a - (N\dot{\phi})_u \right]$ and $\left[(N\dot{\phi})_u - (N\dot{\phi})_b \right]$ respectively in Fig. 2.1(A), diminish with an increasing load. Several explanations have been offered to describe this phenomenon. By assuming a piecewise linear model for the square-loop core, the induced-voltage waveform has been analyzed by graphical construction based on the actual tunnel diode characteristics.[10,11] While these graphical analyses are most effective in determining the amplitude of the constant-voltage plateau $(N\dot{\phi})_u$ in Fig. 2.1(A), they tend to neglect the finer details of the phenomena of spikes and curvatures. The induced-voltage waveform has also been analyzed by reducing the inverter system equations into a single Rayleigh's equation based on a polynomial approximation of the tunnel diode characteristics.[12] In this analysis, the mathematical model defines a single limit cycle of load voltage versus flux for variable line and load conditions of the inverter, leading to the inaccurate conclusion of constant amplitudes for

$(N\dot{\phi})_a$ and $(N\dot{\phi})_b$ in Fig. 2.1(A) that are independent of the input voltage and the output load.

The understanding of the zero-voltage step in Fig. 2.1(B) is very important from an efficiency viewpoint. Large current drawn from the power source during this time interval of almost zero induced voltage reduces considerably the inverter efficiency. This stepped waveform has been observed and documented in a number of reports,[8,9] but none has presented a satisfactory analysis which physically explains the presence of the unwanted step and mathematically calculates it.

In this chapter, the steady-state performances of the inverter including the spikes, the curvatures, and the steps, are analyzed by using a combined graphical and analytical technique. The occurrence of the step is attributed to the inadvertent existence of small source inductance in the low-voltage dc source supplying power to the inverter. Formulas are derived for the purpose of calculating the time intervals of the zero-voltage steps, which show that the length of the step is a direct function of source inductance. The spikes and curvatures are found to be closely related to the inherent nonlinear tunnel diode characteristics and the current continuity required by the saturated core and/or the source inductance. Both are calculated numerically for specific line and load conditions with regard to their amplitudes and time intervals.

Inverter Circuit and System Equations

Figure 2.2 shows the Marzolf tunnel diode inverter with the idealized square-loop core characteristic. Resistance R is the lumped resistance for primary winding N, the viewing resistor, and the connecting leads. The elements R_s and L_s are the internal impedance of the source supplying E_i. The inverter has an output winding of N_L turns and a load resistance R_L. The windings are assumed to have a unity coupling factor, i.e., negligible leakage inductance. The actual components of the test circuit used in this chapter are given in Table I. The nonlinear characteristic of the tunnel diode is shown in the oscillogram of Fig. 2.3.

The system equations are:

$$E_i - i_1R - v_1 - N\dot{\phi} - (i_1 + i_2)R_s - L_s(\dot{i}_1 + \dot{i}_2) = 0 \qquad (1)$$

$$E_i - i_2R - v_2 + N\dot{\phi} - (i_1 + i_2)R_s - L_s(\dot{i}_1 + \dot{i}_2) = 0 \qquad (2)$$

$$i_L = N_L\dot{\phi}/R_L \qquad (3)$$

where $R_L \neq 0$. For convenience, let ΣNi be the net mmf acting on the core at any instant. Thus,

$$\Sigma Ni = N(i_1 - i_2) - N_L i_L \qquad (4)$$

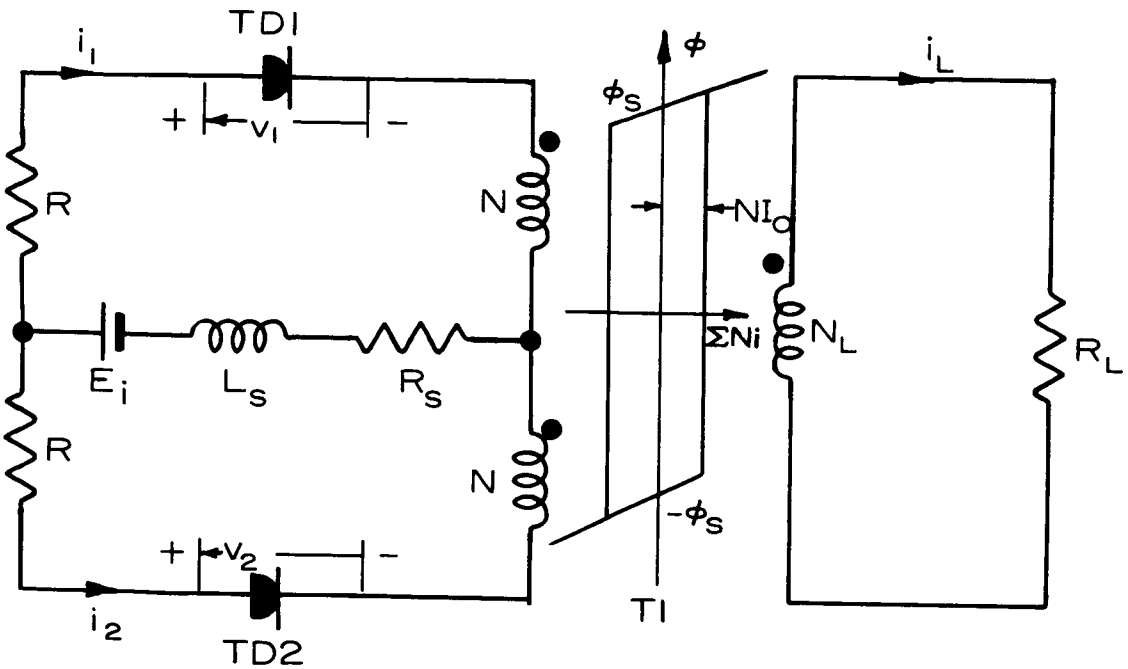


Fig. 2.2. Marzolf Tunnel Diode Inverter Circuit.

TABLE I

Actual Components for Fig. 2.2

N	:	50 turns, #21 AWG
N_L	:	50 turns, #21 AWG
R	:	1 ohm
T1	:	50034-ID, Magnetics, Inc.,
		80% nickel-iron alloy
		ID = 0.75 in.
		OD = 1.125 in.
		HT = 0.375 in.
TD1, TD2	:	1N3150, G.E.
E_i, L_s, R_L, R_s	:	Adjustable

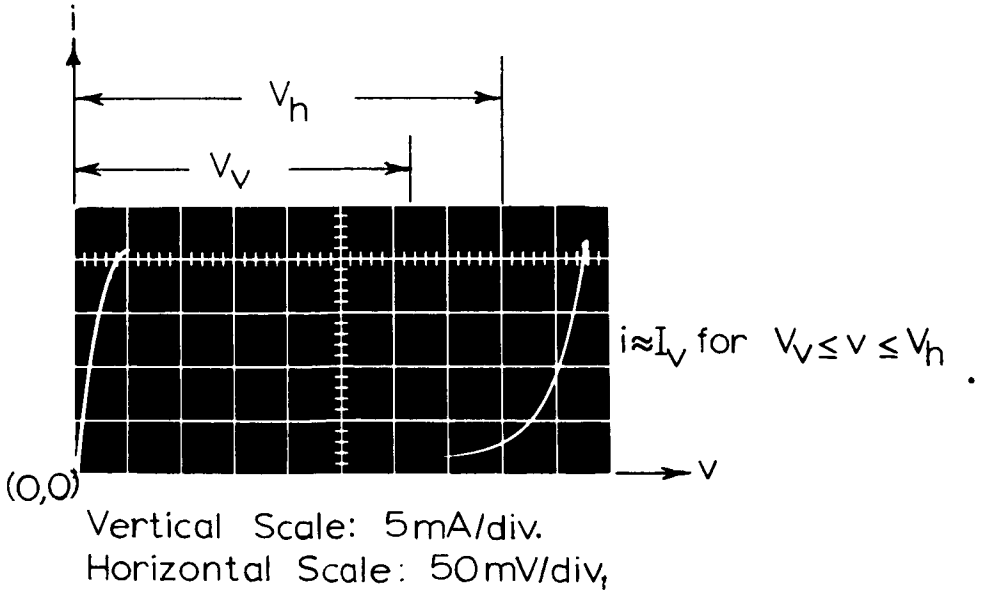


Fig. 2.3. Nonlinear i-v Characteristic of 1N3150.

Here, Σ Ni is the exciting mmf with reference to the primary side of the transformer. In the particular case when the core is unsaturated and $N\dot{\phi} > 0$, Σ Ni equals a constant value NI_o as that indicated in Fig. 2.2. The above four equations, together with the two tunnel diode characteristics, can be used to solve for the instantaneous values of the six variables, namely, i_1, i_2, i_L, v_1, v_2, and $\dot{\phi}$.

Existence of Singular Points

For a given inverter operating under specified conditions, the singular points are defined here as the operating points of the two tunnel diodes on their respective i-v characteristics at which the derivatives of all six variables i_1, i_2, i_L, v_1, v_2, and $\dot{\phi}$ are zero. The following derivation shows that singular-point operation of the inverter occurs only when the square-loop core is unsaturated.

Let K_x be the slope of the ϕ vs. Σ Ni characteristic for the square-loop core. Here, $K_x = \infty$ when the core is unsaturated (i.e., $\frac{d\Sigma Ni}{dt} = 0$), and $K_x = K$ when the core is saturated. Then,

$$\dot{\phi} = \frac{d\phi}{d\Sigma Ni} \frac{d\Sigma Ni}{dt} = K_x\left[N(\dot{i}_1 - \dot{i}_2) - N_L\dot{i}_L \right] \qquad (5)$$

Differentiate the difference of equations (1) and (2),

$$2N\ddot{\phi} = \dot{v}_2 - \dot{v}_1 + R(\dot{i}_2 - \dot{i}_1) \qquad (6)$$

Also, differentiate equation (3) and combine with equations (5) and (6),

$$\frac{\dot{\phi}}{K_x} = \frac{(2N^2R_L + N_L{}^2R)\bullet(\dot{i}_1 - \dot{i}_2) + N_L{}^2(\dot{v}_1 - \dot{v}_2)}{2NR_L} \qquad (7)$$

where $R_L \neq 0$. At singular-point operations the right-hand side of equation (7) vanishes according to the definition of singular points. This demands either $\dot{\phi}$ be zero or K_x be infinity on the left-hand side of equation (7). Since zero $\dot{\phi}$ happens only when a short circuit exists across the load, and thus cannot be regarded as part of the normal inverter operation, the only possibility for singular points to exist is to have an infinite K_x. Since the definition of K_x is $d\phi/d\,\Sigma Ni$, $K_x = \infty$ means that the flux excursions of the square-loop core under this condition are limited on one or the other of the two vertical unsaturated segments of its idealized ϕ vs. ΣNi characteristic. The induced voltage corresponding to singular-point operation is $(N\dot{\phi})_u$ of the constant-voltage plateau between points u and w of Fig. 2.1(A).

Graphical Determination of the Singular Points

From equations (3) and (4), and remembering that during singular-point operation Σ Ni is equal to NI_o when $N\dot{\phi} > 0$,

$$(N\dot{\phi}/R_L') + I_o = I_1 - I_2 \qquad (8)$$

where $R_L' = (N/N_L)^2 R_L$ is the equivalent load resistance reflected from the secondary to the primary side. Here, I_1 and I_2 are used to replace i_1 and i_2 of equation (4) to symbolize the constant currents at singular-point operations. From equations (1), (2), and (8), and remembering $\dot{i}_1 = \dot{i}_2 = 0$ for singular-point operations,

$$(E_i + I_o R_s) - V_1 - I_1(R + 2R_s) - (N\dot{\phi})_u\left(1 - \frac{R_s}{R_L'}\right) = 0 \qquad (9)$$

$$(E_i - I_o R_s) - V_2 - I_2(R + 2R_s) + (N\dot{\phi})_u\left(1 - \frac{R_s}{R_L'}\right) = 0 \qquad (10)$$

For a given inverter with specified E_i and R_L, equations (8), (9), and (10), together with the two tunnel diode characteristics, are used to solve for the five unknowns V_1, V_2, I_1, I_2, and $(N\dot{\phi})_u$ through the graphical analysis illustrated in Fig.

2.4. Points s1 and s2 in the figure are singular points. The sequence of graphical analysis is as follows:

(1) Start with an arbitrarily chosen $N\dot{\phi}$, locate $E_i + I_o R_s - N\dot{\phi}(1 - \frac{R_s}{R_L'})$ and $E_i - I_o R_s + N\dot{\phi}(1 - \frac{R_s}{R_L'})$ on the voltage axis.

(2) From each of the two intersections on the voltage axis draw a straight line of slope $-(R + 2R_s)^{-1}$ to intersect the diode characteristics at the low- and high-voltage positive-resistance segments respectively.

(3) Check to see if equation (8) is satisfied.

(4) If not, keep on changing $N\dot{\phi}$ in step (1) and repeat steps (2) and (3) until equation (8) is satisfied at a certain $N\dot{\phi}$. The particular $N\dot{\phi}$ corresponds to the induced voltage at singular-point operation when the core is unsaturated, and is denoted hereafter by $(N\dot{\phi})_u$.

Using the method outlined in this section, singular points for different line and load conditions are obtained for the test circuit. As can be seen from the theoretical results given in Fig. 2.5, they are in good agreement with the experimental values.

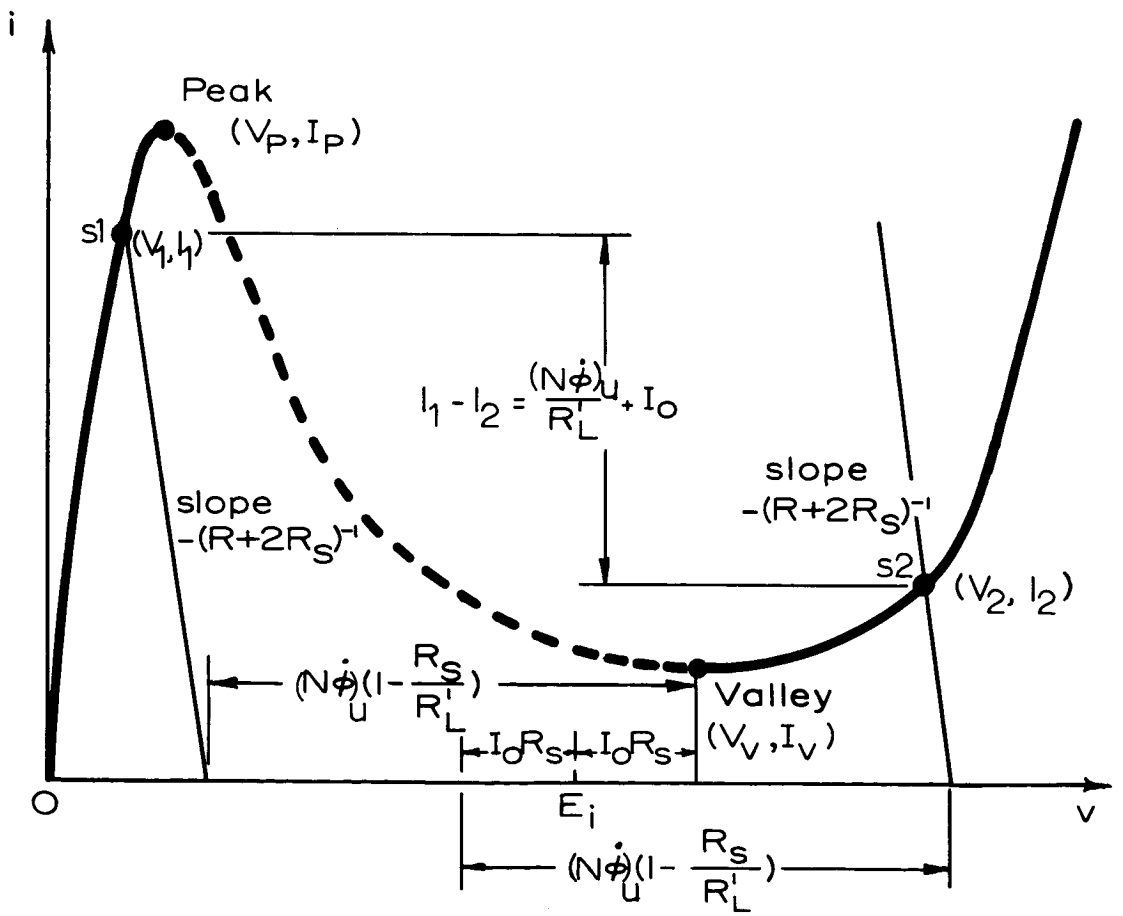


Fig. 2.4. Graphical Construction of Singular Points.

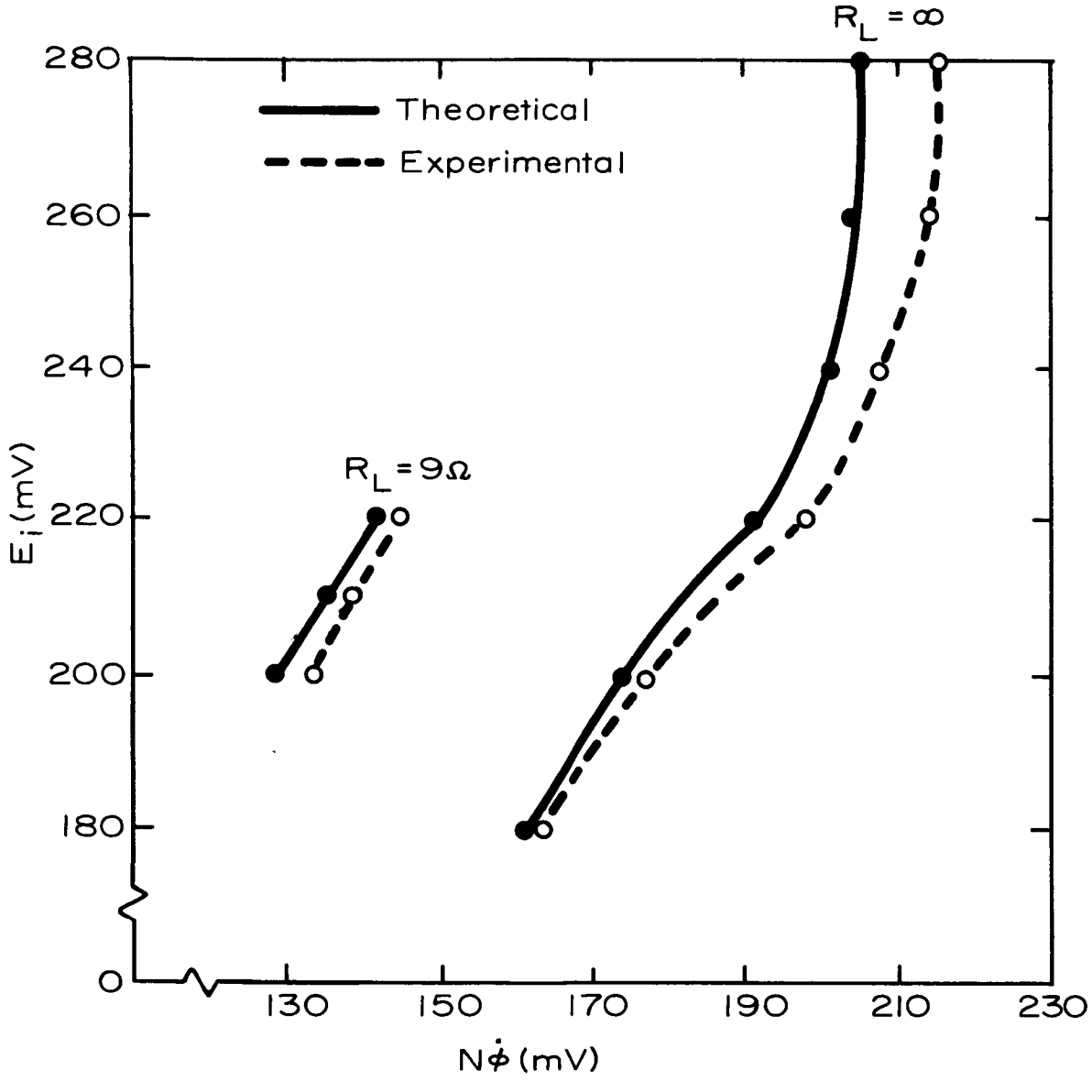


Fig. 2.5. Input Voltage vs. Induced Voltage at Singular-Point Operations.

Conditions of Non-Existence of Singular Points

As can be seen from Fig. 2.4, the singular points s1 and s2 of the two diodes locate on the two positive-resistance segments where $V_1 < V_p$ and $V_2 > V_v$. From the diagram it is obvious that the singular points s1 and s2 migrate up and down the respective tunnel diode characteristics with variable line and load conditions. As long as the two singular points are located within the respective positive-resistance segments, square-wave induced voltages such as that shown in Fig. 2.1(A) are generated across all the windings. If, due to either inadequate input voltage or inadequate load one of these two singular points is located in the negative-resistance region, abnormal high-frequency oscillation then occurs.[13] From Fig. 2.4, this arises in any of the following conditions:

(1) For a given load resistance, the input voltage is so low that for $V_2 > V_v$ in Fig. 2.4, the current difference $(I_1 - I_2)$ is less than $\left[(N\dot{\phi})_u/R_L'\right] + I_o$ in equation (8).

(2) For a given load resistance, the input voltage is so high that for $V_1 < V_p$ in Fig. 2.4, the current difference $(I_1 - I_2)$ is less than $\left[(N\dot{\phi})_u/R_L'\right] + I_o$ in equation (8).

(3) For a given input voltage, the load resistance is so small that for $V_1 < V_p$ and $V_2 > V_v$ in Fig. 2.4, the current difference $(I_1 - I_2)$ is less than $\left[(N\dot{\phi})_u/R_L'\right] + I_o$ in equation (8).

The theoretical and experimental domains of normal operations are shown in Fig. 2.6. Any combination of E_i and R_L above the U-shaped curve results in normal operation for the inverter.

Degree of Saturation of the Core

Figure 2.7(A) shows in detail the idealized square-loop characteristic of the core with $K_x = \infty$ for the unsaturated regions and $K_x = K$ for the saturated regions. The net mmf acting on the core can be expressed as:

$$\Sigma Ni = N \left(i_1 - i_2 - \frac{N\dot{\phi}}{R_L'}\right) \qquad (11)$$

where $i_1 - i_2 - \frac{N\dot{\phi}}{R_L'} = I_o$ for the particular case when the core is unsaturated and $N\dot{\phi} > 0$. After the core saturates at point w, the singular-point operation of the inverter ceases. The value of ΣNi begins to increase from the constant unsaturated value NI_o. This increasing mmf causes i_1 and i_2 to move in the direction of I_p and I_v respectively. During this time of increasing i_1 and decreasing i_2, the terms $L_s (\dot{i}_1 + \dot{i}_2)$ in equations (1) and (2) are no longer zero. To determine the effect of $L_s (\dot{i}_1 + \dot{i}_2)$, assume the inverter is operating at no load. Whether the voltage $L_s(\dot{i}_1 + \dot{i}_2)$ is negligible or not depends on its amplitude as compared to the induced voltage

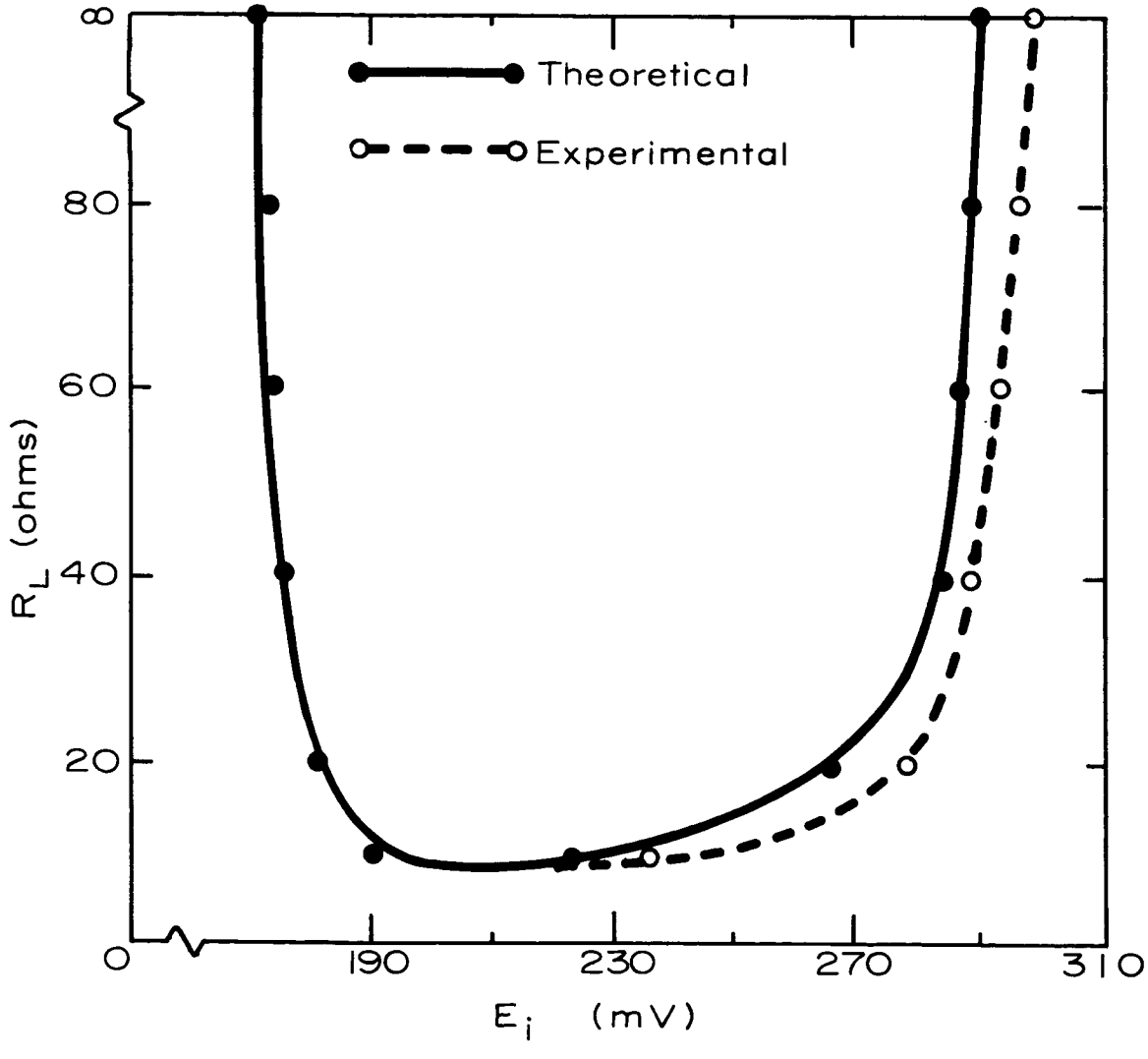


Fig. 2.6. Domain of Normal Operation.

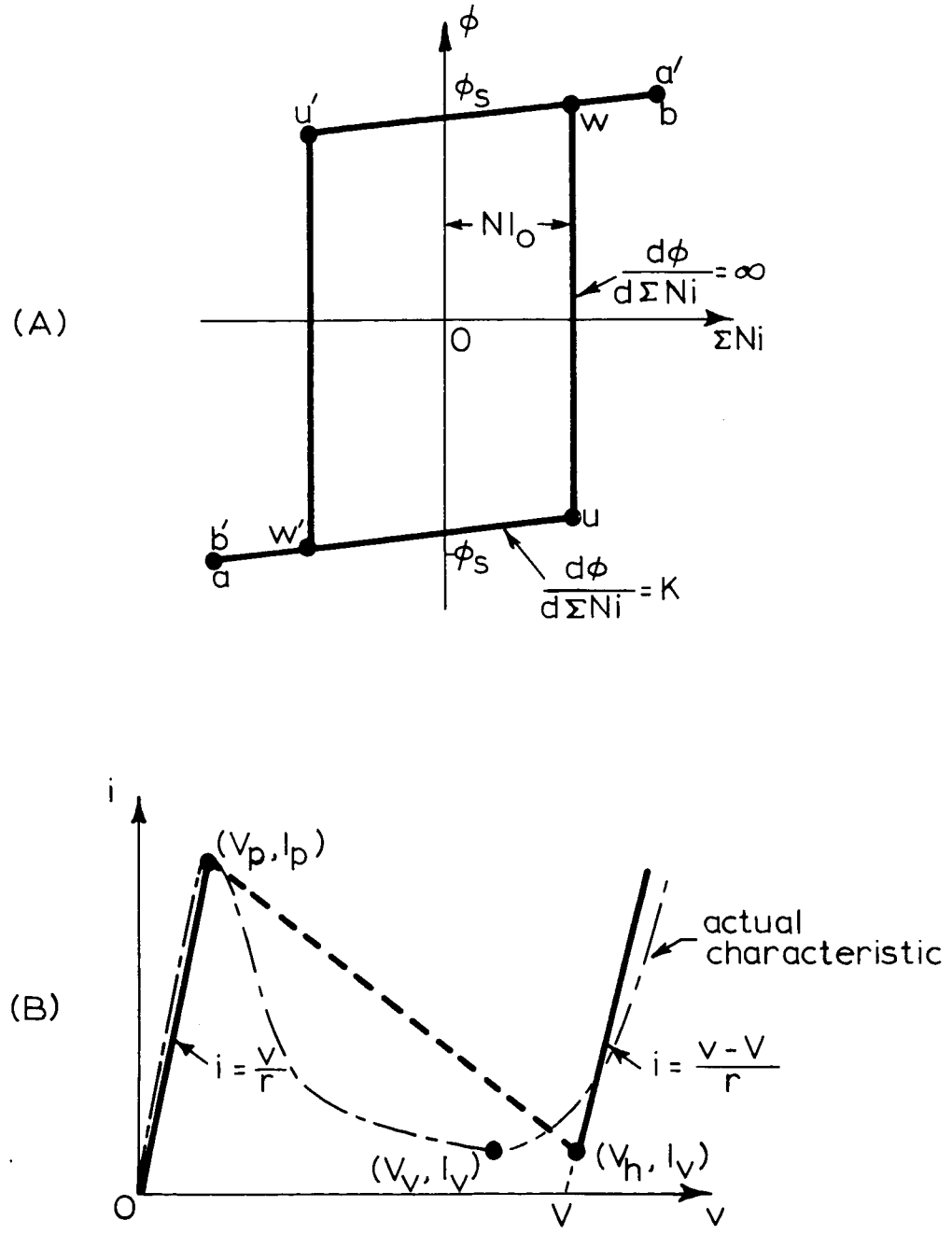


Fig. 2.7. Idealized Square-Loop Core and Tunnel Diode Characteristics.

$N\dot{\phi} = L_w(i_1 - i_2)$, where $L_w = N^2K$ is the self inductance of the primary winding of the saturated core. Normally, L_w is much greater than L_s. Also, $|\dot{i}_1 - \dot{i}_2|$ is larger than $|\dot{i}_1 + \dot{i}_2|$ due to the opposite sign associated with $\dot{i}_1$ and $\dot{i}_2$ between points w and b. Consequently, the effect of source inductance on the operation of the inverter between w and b is neglected. Mathematical proof of the same fact is provided by the derivations of Appendix A, in which the idealized tunnel diode characteristic of Fig. 2.7(B) is used.

The degree of saturation of the core, i.e., the position of point b, is determined by the maximum ΣNi in equation (11). With respect to the tunnel diode characteristics, this maximum ΣNi occurs when either the peak or the valley of any one diode is reached. With negligible effect of L_s between w and b and the additional assumption of negligible R_s, the maximum ΣNi at point b of Fig. 2.7(A) can then be calculated from equation (11) under the conditions specified either by Fig. 2.8(A) when $E_i < (V_p + V_v)/2$ where the valley is reached first or by Fig. 2.8(B) when $E_i > (V_p + V_v)/2$ where the peak is reached first. Here, the point b corresponds to the same point on Fig. 2.7(A), and numbers "1" and "2" are used to symbolize diode #1 and #2 respectively.

From the above discussion, the sequence of graphical analysis for the maximum ΣNi is as follows:

(1) From the peak and the valley, draw straight lines of slope $-(R + 2R_s)^{-1}$ to intersect the voltage axis at two points C and D respectively.

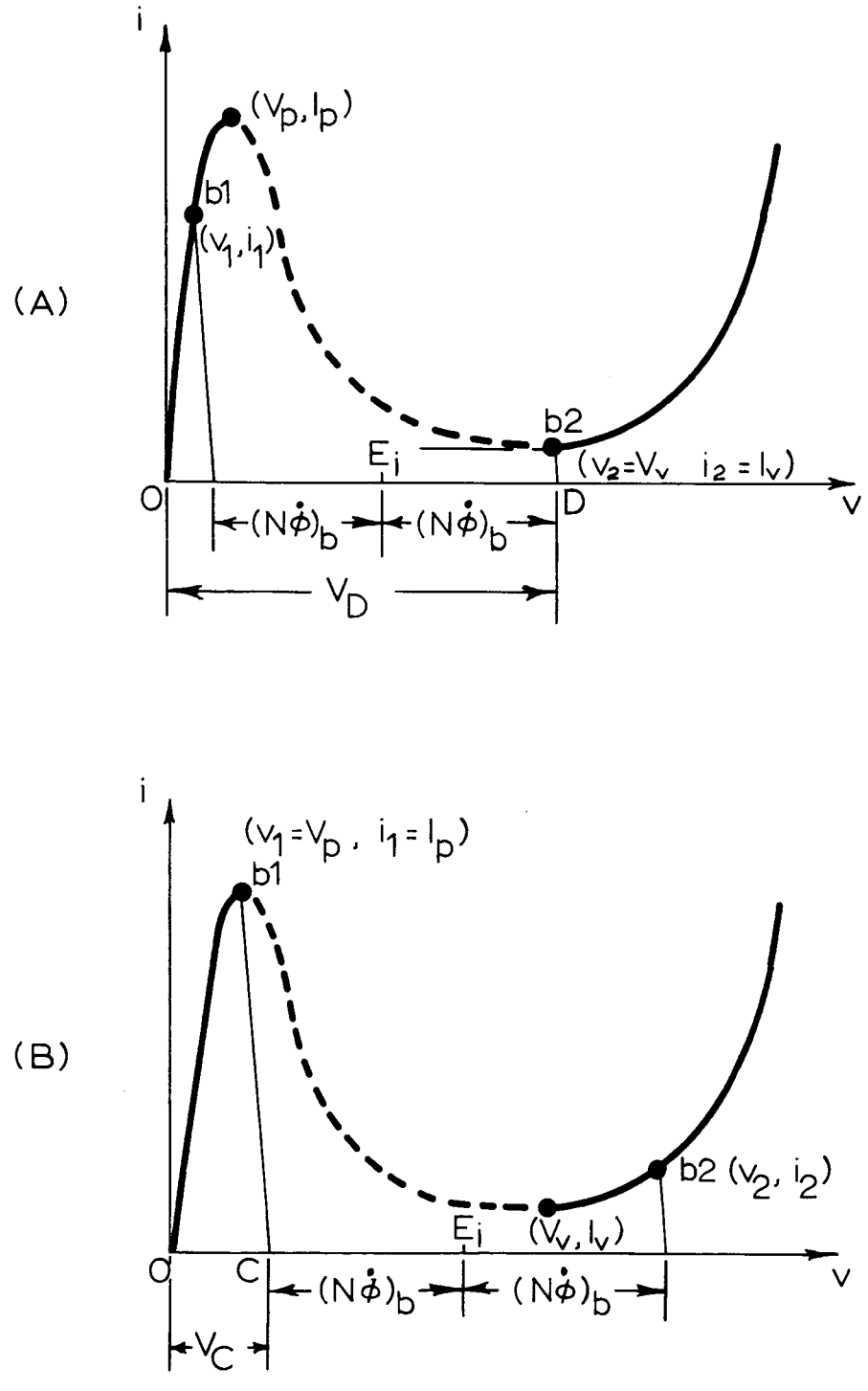


Fig. 2.8. Conditions for Maximum Saturation of the Core.

(A) The Valley Point of One Diode Is Reached First

(B) The Peak Point of One Diode Is Reached First

(2) Compare $(v_D - E_i)$ and $(E_i - v_C)$. The larger voltage difference is $(N\dot{\phi})_b$. If $(v_D - E_i) > (E_i - v_C)$, then Fig. 2.8(A) is used. If $(v_D - E_i) < (E_i - v_C)$, then Fig. 2.8(B) is used.

(3) From E_i and $(N\dot{\phi})_b$, find point b1 in Fig. 2.8(A) when b2 is at the valley or b2 in Fig. 2.8(B) when b1 is at the peak. The maximum ΣNi can then be calculated from equation (11) with the known values of i_1 and i_2, and with $N\dot{\phi}$ replaced by $(N\dot{\phi})_b$.

Inverter Operation Immediately After the Maximum Saturation of the Core

While the effect of L_s is negligible between points w and b, it can be influential to the inverter operation at the instant immediately after b. This is especially true with inverters employing high-current tunnel diodes. To understand this physically, consider the circuit diagram of Fig. 2.2 and the loop equations (1) and (2). For a clearer presentation, neglect the effect of source resistance R_s. Then,

$$E_i - v_1 - i_1R - N\dot{\phi} - L_s(\dot{i}_1 + \dot{i}_2) = 0 \qquad (12)$$

$$E_i - v_2 - i_2R + N\dot{\phi} - L_s(\dot{i}_1 + \dot{i}_2) = 0 \qquad (13)$$

Here, i_1R and i_2R are normally very small. For illustrative purpose, also consider the circuit conditions as point b2 in Fig. 2.8(A) is about to be reached. These conditions are $i_2 = I_v$, $v_2 = V_v > E_i$, $N\dot{\phi} > 0$, and $L_s(i_1 + i_2) \approx 0$, as explained in the previous section. As soon as point b2 is passed, diode #2 switches instantly across the negative-resistance region to a certain point on its low-voltage positive-resistance segment, causing v_2 to decrease suddenly. Due to the extremely short switching time of the tunnel diode, diode #1 has yet to reach the peak. In order to satisfy equation (13), either $N\dot{\phi} = L_w(\dot{i}_1 - \dot{i}_2)$ must decrease or $L_s(\dot{i}_1 + \dot{i}_2)$ increase suddenly to compensate for the sudden decrease in v_2. Here i_1 and i_2 are the rate of current increases in diode #1 and #2 along the respective low-voltage positive-resistance segment to which diode #2 has just switched. Unlike the situation before the switching of diode #2 when the diodes are on different positive-resistance segments, i.e., when $\dot{i}_1 > 0$ and $\dot{i}_2 < 0$, both $\dot{i}_1$ and $\dot{i}_2$ are positive after the switching of diode #2. Consequently, even when L_s is normally much smaller than L_w, the voltage $L_s(\dot{i}_1 + \dot{i}_2)$ is not necessarily negligible as compared to $N\dot{\phi} = L_w(\dot{i}_1 - \dot{i}_2)$ after the switching takes place. If $L_s(\dot{i}_1 + \dot{i}_2)$ is still smaller than $N\dot{\phi} = L_w(\dot{i}_1 - \dot{i}_2)$, then, $N\dot{\phi}$ of equation (13) changes suddenly to compensate for the change in v_2, which in turn causes a sudden increase in v_1 of equation (12). When this happens, diode #1 suddenly switches, resulting in an almost simultaneous switching for both tunnel diodes. On the other hand, if $L_s(\dot{i}_1 + \dot{i}_2)$ is larger than $N\dot{\phi}$, both diodes will

migrate upward along the respective low-voltage segment following the switching of diode #2 from its valley point to its low-voltage segment. The migration continues until diode #1 reaches its peak and switches toward its high-voltage segment. During this interval when both diodes are on the low-voltage segment, a step of small induced voltage $N\dot{\phi} = L_w(\dot{i}_1 - \dot{i}_2)$ occurs as shown in Fig. 2.1(B).

It is noted that while Fig. 2.8(A) has been used to describe the significance of $L_s\ (\dot{i}_1 + \dot{i}_2)$, similar argument can be applied to Fig. 2.8(B) when diode #1 switches from its peak point toward its high-voltage segment before point b2 of diode #2 reaches its valley. For small $L_s(\dot{i}_1 + \dot{i}_2)$, both diodes switch almost simultaneously as soon as diode #1 passes its peak. For large $L_s(\dot{i}_1 + \dot{i}_2)$, both diodes then stay on the respective high-voltage segment and migrate downward toward the valley until diode #2 reaches its valley, causing a similar small-voltage step in the induced-voltage waveform.

In the following discussions, the voltage spikes and curvatures are analyzed first for the case where $L_s(\dot{i}_1 + \dot{i}_2)$ is small compared to $N\dot{\phi} = L_w(\dot{i}_1 - \dot{i}_2)$. Similar analytic techniques are then modified to treat the case where $L_s(\dot{i}_1 + \dot{i}_2)$ is large compared to $N\dot{\phi} = L_w(\dot{i}_1 - \dot{i}_2)$. Intervals of voltage steps due to both diodes operating on the same respective high- or low-voltage positive-resistance segment are then calculated.

Voltage Spikes and Curvatures for Small $L_s(\dot{i}_1 + \dot{i}_2)$

As explained in the previous section, both diodes switch almost simultaneously in case of small $L_s(\dot{i}_1 + \dot{i}_2)$. For illustrative purpose, Fig. 2.9 demonstrates in detail the conditions of Fig. 2.8(B) where diode #1 arrives at the peak before diode #2 reaches the valley. The effect of source resistance is again neglected in favor of a clearer presentation. Equations (12) and (13) are then used for the graphical analysis of Fig. 2.9. Points "s" are "singular" points. Points "b" and "a" are the operating points instantly "before" and instantly "after" the switching of both diodes. Postscripts "1" and "2" refer to diodes #1 and #2 respectively. The induced voltage at singular-point operation is $(N\dot{\phi})_u$ when the core is unsaturated. After the core saturates, currents i_1 and i_2 begin to move in the direction of I_p and I_v respectively. Meanwhile, the induced voltage decreases from the singular-point value toward $(N\dot{\phi})_b$, at which point i_1 becomes I_p. The subscript "b" in $(N\dot{\phi})_b$ is again used to symbolize the induced voltage just before the switching of tunnel diode #1. At this instant, equation (11) can be written as

$$(\Sigma Ni)_b = N(i_1 - i_2)_b - \frac{N(N\dot{\phi})_b}{R_L'} \qquad (14)$$

With the saturated core acting as an inductor with inductance

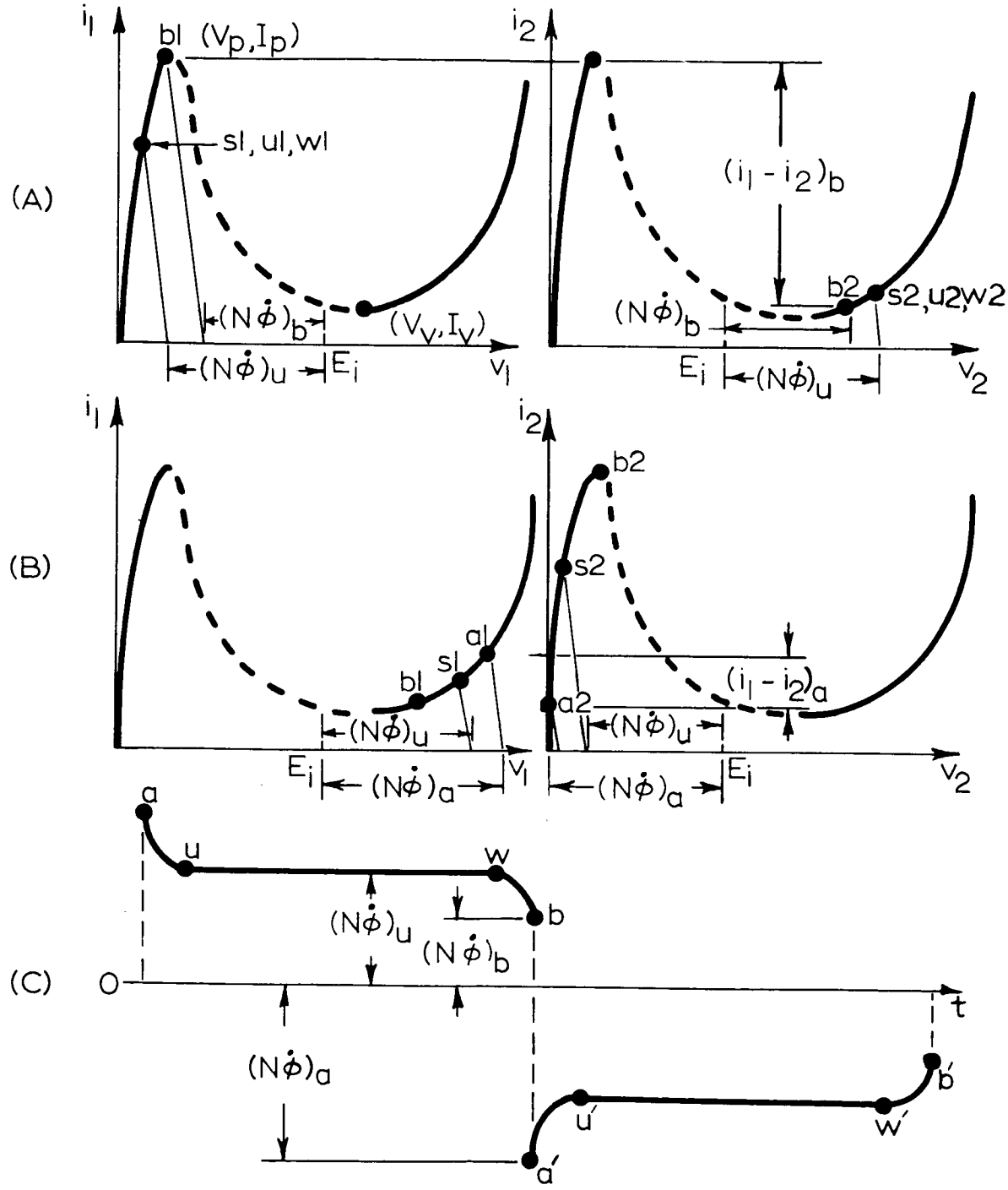


Fig. 2.9. Operation of Tunnel Diodes and the Induced-Voltage Waveform.

(A) Before the Switching
(B) After the Switching
(C) The Corresponding Induced-Voltage Waveform

L_w ($>> L_s$) whose mmf cannot change instantaneously, the almost zero switching time of the tunnel diodes requires that this value of $(\Sigma Ni)_b$ must be maintained at the instant immediately after the switching of both diodes. Let $(N\dot{\phi})_a$ be the induced voltage just "after" the switching, then,

$$(\Sigma Ni)_a = (\Sigma Ni)_b = N(i_1 - i_2)_a - \frac{N(N\dot{\phi})_a}{R_L'} \qquad (15)$$

Therefore,

$$(i_1 - i_2)_b - \frac{(N\dot{\phi})_b}{R_L'} = (i_1 - i_2)_a - \frac{(N\dot{\phi})_a}{R_L'} \qquad (16)$$

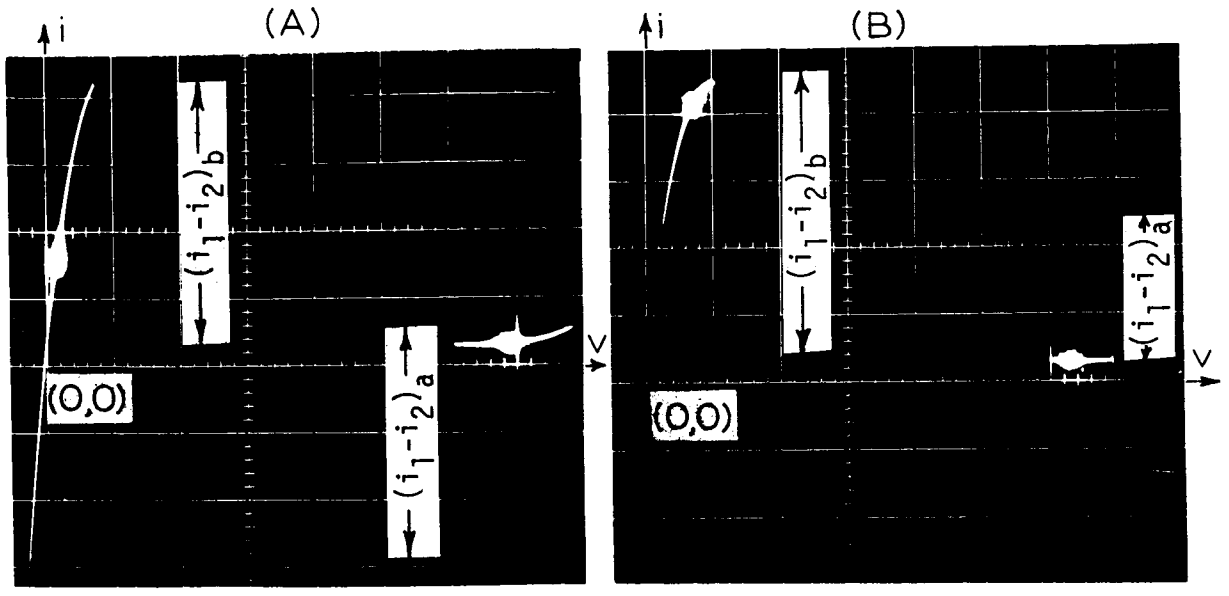
It is noted that the algebraic sign associated with $(N\dot{\phi})_a$ is the opposite of that of $(N\dot{\phi})_b$. This is evident if equation (2) is subtracted from equation (1). Here, $N\dot{\phi} \approx (v_2 - v_1)/2$ since voltage drops i_1R and i_2R are normally negligible. As can be seen from Fig. 2.9(A) and (B), $(N\dot{\phi})_b \approx (v_2 - v_1)_b/2 > 0$, and $(N\dot{\phi})_a \approx (v_2 - v_1)_a/2 < 0$. Numerically, equation (16) thus becomes:

$$(i_1 - i_2)_b - \left|\frac{(N\dot{\phi})_b}{R_L'}\right| = (i_1 - i_2)_a + \left|\frac{(N\dot{\phi})_a}{R_L'}\right| \qquad (17)$$

For a given inverter with specific line and load conditions, both $(i_1 - i_2)_b$ and $(N\dot{\phi})_b$ can be found by the graphical analysis described earlier and illustrated in Fig. 2.9(A), using the actual tunnel diode characteristics. With the left-hand side of equation (17) now a known quantity, a few trials of different values for $(N\dot{\phi})_a$ are sufficient to match both sides of equation (17) through the graphical technique illustrated in Fig. 2.9(B). Thus, the induced voltage $(N\dot{\phi})_a$ and the operating points a1 and a2 immediately after the switching are obtained.

From equation (17), the maximum $(i_1 - i_2)_a$ occurs at no load when it is equal to $(i_1 - i_2)_b$. The induced voltage $(N\dot{\phi})_a$ is also maximum at no load as can be seen from Fig. 2.9(B) since the difference in current $(i_1 - i_2)_a$ increases with the induced voltage $(N\dot{\phi})_a$. Consequently, the amplitude of $(N\dot{\phi})_a$ diminishes with an increasing load. As is evident from Fig. 2.4, the increasing load (i.e., smaller R_L') also causes the singular points s1 and s2 to move closer toward the peak of one diode and the valley of the other diode, thereby reducing the difference between $(N\dot{\phi})_u$ and $(N\dot{\phi})_b$. As is shown in the induced-voltage waveform of Fig. 2.9(C), the difference between $(N\dot{\phi})_a$ and $(N\dot{\phi})_u$ appears as a voltage spike, while that between $(N\dot{\phi})_u$ and $(N\dot{\phi})_b$ as a voltage curvature. Consequently, the increasing load results in a higher-quality square-wave output.

Because of the two closely-matched tunnel diodes used in the inverter, oscillograms in Fig. 2.10 represent the



Vertical Scale: 5mA/div.
Horizontal Scale: 50mV/div.

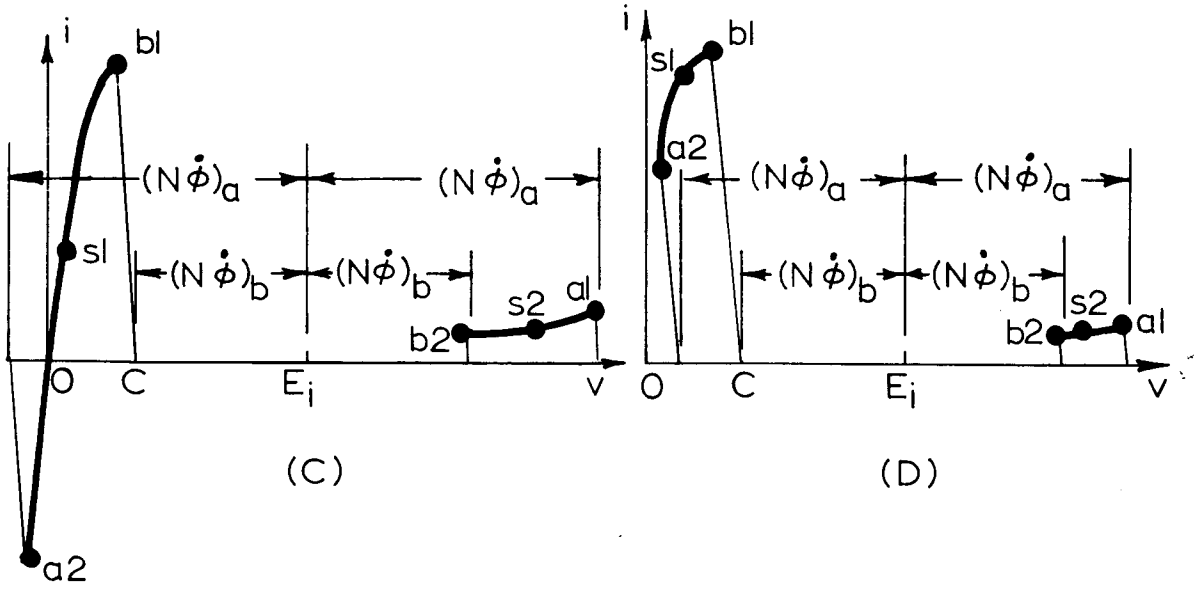


Fig. 2.10. Oscillograms of i-v Operating Characteristics of Tunnel Diodes.

(A) E_i = 200 mV, $R_L = \infty$, R_s = 0
(B) E_i = 200 mV, R_L = 10 ohms, R_s = 0
(C) Explanation for (A)
(D) Explanation for (B)

operating characteristics of any one of the two tunnel diodes for two different load conditions. The bright spots on the oscillograms are the singular points when the core is unsaturated. Notice that in Fig. 2.10(A) under no-load condition, the two current differences before and after the switching of the tunnel diodes are identical, as demanded by equation (17) when $R_L' = \infty$. Also, the diode current becomes negative in this particular case in order to satisfy equation (17). Figure 2.10(B) is for heavy-load condition. The differences between i_1 and i_2 before and after the switching are no longer the same, due to the effects of $|(N\dot{\phi})_a/R_L'|$ and $|(N\dot{\phi})_b/R_L'|$ in equation (17). Numerical calculations for the cases corresponding to the oscillograms (A) and (B) are carried out and illustrated with the sketches in (C) and (D). The letters s, b, and a are again used to symbolize the singular points, the operating points instantly before, and the operating points instantly after the switching of tunnel diodes. The graphical analysis of Fig. 2.10(C) yields the following results: $(i_1 - i_2)_b$ = 20 mA and $(N\dot{\phi})_b$ = 115 mV. From equation (17) and the experimentally-determined tunnel diode characteristic shown in Fig. 2.3, computation yields a value of 20 mA for $(i_1 - i_2)_a$ and 240 mV for $(N\dot{\phi})_a$. This value of $(N\dot{\phi})_a$ is greater than the input voltage E_i = 200 mV, resulting in a negative diode current instantly after the switching. In Fig. 2.10(D), similar calculations indicate that $(i_1 - i_2)_b$ = 20 mA, $(N\dot{\phi})_b$ = 135 mV, $(i_1 - i_2)_a$ = - 8.5 mA, and $(N\dot{\phi})_a$ = 170 mV. In the oscillograms of Fig. 2.10, only the operating i-v characteristics before and

after the switching are visible. The part of the operating characteristic during the switching is not discernible, due to the extremely fast switching speed of the tunnel diodes.

Using the method outlined in this section, the theoretical values of $(N\dot{\phi})_a$, $(N\dot{\phi})_b$, and $(N\dot{\phi})_u$ of Fig. 2.1(A) for different line and load conditions with $R_s = 0$ are calculated. The corresponding experimental values are shown in the oscillograms of Fig. 2.11. The line and load conditions of Fig. 2.11(A) are identical to those of Fig. 2.10(A). The numbers in the parentheses are theoretical values. They are in good agreement with the experimental ones measured directly from the oscillograms. The fact that all calculated voltages are consistently smaller than the corresponding experimental ones suggests a certain source of error, which could be a slightly-inaccurate tunnel diode characteristic employed by the graphical analysis.

Determination of Period, $L_s(\dot{i}_1 + \dot{i}_2)$ Negligible

An idealized core characteristic was shown earlier in Fig. 2.7(A). The points located around the loop correspond to those on Fig. 2.9(C). There are three time intervals associated with one half cycle of the induced-voltage waveform; namely, T_{au}, T_{uw}, and T_{wb}.

The Numbers Inside the Parentheses are Calculated Values.

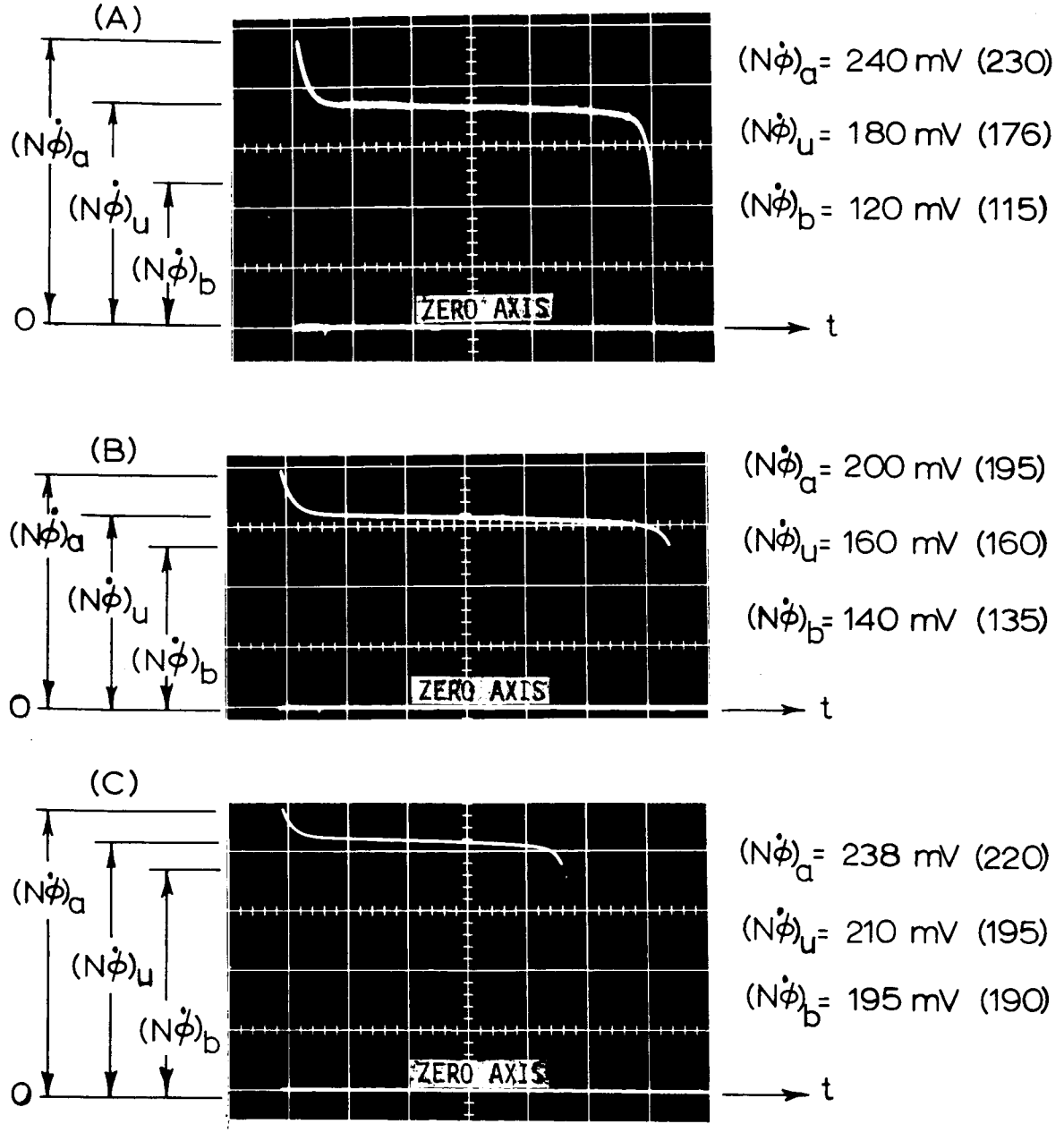


Fig. 2.11. Oscillograms of Induced-Voltage Waveform, $L_s = 0$.

(A) E_i = 200 mV, $R_L = \infty$, R_s = 0, L_s = 0

(B) E_i = 180 mV, R_L = 110 ohms, R_s = 0, L_s = 0

(C) E_i = 280 mV, R_L = 40 ohms, R_s = 0, L_s = 0

Within the interval T_{uw}, the induced voltage $(N\dot{\phi})_u$ when K_x is infinite has been obtained from the graphical analysis of singular points. Therefore,

$$T_{uw} = 2N\phi_s/(N\dot{\phi})_u \tag{18}$$

where ϕ_s is the saturation flux level of the core.

Time intervals T_{au} and T_{wb} associated with the spikes and the curvatures are more difficult to calculate as the operating points of both diodes are no longer fixed at the singular points as they were during T_{uw}, but are now migrating along the respective nonlinear i-v characteristics of the tunnel diodes. However, approximate calculations for these time intervals can be made by assigning to both diodes the ideal N-shaped characteristic such as that shown in Fig. 2.7(B) where the two positive-resistance segments are assumed to have the same slope r. Equations for the low- and high-voltage segments are then v = ir and v = V + ir, respectively.

Substituting $i_1 r$ for v_1 and $V + i_2 r$ for v_2, and differentiating equations (3), (12), and (13), the following expressions for $\dot{i}_1$, $\dot{i}_2$, and $\dot{i}_L$ are derived:

$$\dot{i}_1 = - N\ddot{\phi}/(R + r) \tag{19}$$

$$\dot{i}_2 = N\ddot{\phi}/(R + r) \tag{20}$$

$$\dot{i}_L = N_L\ddot{\phi}/R_L \tag{21}$$

Substituting the above three equations into equation (5) with $K_x = K$ for the saturated core,

$$\ddot{\phi} + (\dot{\phi}/G) = 0 \tag{22}$$

where

$$G = N^2K\left(\frac{2}{R + r} + \frac{1}{R_L'}\right) = L_w\left(\frac{2}{R + r} + \frac{1}{R_L'}\right) \tag{23}$$

As determined in the previous section, the initial and final induced voltages for time interval T_{au} are $(N\dot{\phi})_a$ and $(N\dot{\phi})_u$, and for time interval T_{wb} are $(N\dot{\phi})_u$ and $(N\dot{\phi})_b$. Consequently, from equation (22),

$$T_{au} + T_{wb} = G \ln \frac{(N\dot{\phi})_a}{(N\dot{\phi})_u} + G \ln \frac{(N\dot{\phi})_u}{(N\dot{\phi})_b} = G \ln \frac{(N\dot{\phi})_a}{(N\dot{\phi})_b} \tag{24}$$

Upon combining equations (18) and (24), the period T for a complete cycle is:

$$T = 2(T_{au} + T_{uw} + T_{wb}) = \frac{4N\phi_s}{(N\dot{\phi})_u} + 2G \ln \frac{(N\dot{\phi})_a}{(N\dot{\phi})_b} \qquad (25)$$

For a good quality of square-wave voltage, it is desirable to have both T_{au} and T_{wb} short and the difference between $(N\dot{\phi})_a$ and $(N\dot{\phi})_b$ small. This requires that the ratios of $(N\dot{\phi})_a$ to $(N\dot{\phi})_u$ and $(N\dot{\phi})_u$ to $(N\dot{\phi})_b$ be close to unity, which is generally approached when the output load becomes larger.

Equations (18) and (24) are used to calculate the period for the three different line and load conditions specified earlier in Fig. 2.11. For the inverter test circuit, the following parameters are used: $\phi_s = 1.9 \times 10^{-5}$ webers, $K = 3.6 \times 10^{-6}$ weber/amp-turn, r = 3 ohms, and R = 1 ohm. Consequently, the factor G is approximately 4.5×10^{-3} for all three conditions of Fig. 2.11. The calculated values of T_{uw} and $T_{au} + T_{wb}$ are listed below inside the parentheses. For comparative purposes, the experimental time intervals are read directly from the oscillograms of Fig. 2.11, and placed before the parentheses.

For Fig. 2.11(A), T_{uw} = 10 ms (10.9 ms)

$T_{au} + T_{wb}$ = 2 ms (2.8 ms)

For Fig. 2.11(B) T_{uw} = 11.2 ms (12.0 ms)

$T_{au} + T_{wb}$ = 1.3 ms (1.7 ms)

For Fig. 2.11(C) T_{uw} = 8 ms (9.7 ms)

$T_{au} + T_{wb}$ = 1.1 ms (0.7 ms)

The calculated time intervals for Fig. 2.11(A) and (B) are longer than the experimental ones. This is because of the consistently smaller values of induced voltages calculated in the previous section, as these values are the ones used in equations (18) and (24) of this section for calculating the time intervals. The relatively larger difference between the calculated and experimental T_{uw} in Fig. 2.11(C) is attributed to the relatively larger difference between the calculated and experimental $(\dot{N\phi})_u$ of the previous section. The fact that the theoretical $T_{au} + T_{wb}$ of Fig. 2.11(C) is shorter than the experimental one whereas those of Fig. 2.11(A) and (B) are longer can be explained by the relatively large difference between the theoretical and experimental $(\dot{N\phi})_a/(\dot{N\phi})_b$, as the theoretical one is used in equation (24) for calculating $T_{au} + T_{wb}$. Numerically, the ratios of theoretical $(\dot{N\phi})_a/(\dot{N\phi})_b$ to experimental $(\dot{N\phi})_a/(\dot{N\phi})_b$ for Fig. 2.11(A), (B), and (C) are 1, 1.011, and 0.949, respectively.

Voltage Spikes and Curvatures, Large $L_s(\dot{i}_1 + \dot{i}_2)$

In this section, the effect of large $L_s(\dot{i}_1 + \dot{i}_2)$ to the inverter operation is discussed. First, the alternate switching of the diodes at the peak and the valley point along a constant-current path when $L_s(\dot{i}_1 + \dot{i}_2)$ is large is explained. This property of constant-current switching is then utilized to calculate rather accurately the voltage spikes and curvatures regardless of the large amplitude of $L_s(\dot{i}_1 + \dot{i}_2)$.

As described earlier in this chapter, if the effect of $L_s(\dot{i}_1 + \dot{i}_2)$ is negligible, and the inverter is assumed operating at no load, it is pointed out that the current difference $(i_1 - i_2)$ remains unchanged before and after the switching of both diodes. However, if the effect of $L_s(\dot{i}_1 + \dot{i}_2)$ is significant due to a large L_s and/or a large $(\dot{i}_1 + \dot{i}_2)$, the requirement that the source current $(i_1 + i_2)$ cannot change instantaneously becomes quite influential. Thus, neither i_1 nor i_2 can change suddenly due to the requirement for their sum and for their difference to be continuous. Consequently, the switching of either diode across its respective negative-resistance region is accomplished along a path of constant current.

In an earlier section of this chapter where the inverter operation immediately after maximum saturation of the core is discussed, it is pointed out that following the switching of one of the two diodes across its negative-resistance region, the effect of a large $L_s(\dot{i}_1 + \dot{i}_2)$ is to cause both diodes to stay on the same positive-resistance segment. Currents in both

diodes then either increase or decrease simultaneously along the same voltage segment of their respective characteristics, resulting in an interval during which the induced voltage is small. This interval continues until the other diode reaches its peak or its valley and switches across its negative-resistance region.

To sum up the discussions, while $L_s(\dot{i}_1 + \dot{i}_2)$ is relatively small during the intervals when the diodes are operating on the respective different voltage segments where $\dot{i}_1$ and $\dot{i}_2$ have opposite sign, it is not necessarily small during the interval when both diodes are operating on the same voltage segment where $\dot{i}_1$ and $\dot{i}_2$ have the same sign. In the later case, the fact that neither i_1 nor i_2 can change suddenly requires that the diodes must switch at the peak or the valley point along a constant-current path.

Figure 2.12 shows two oscillograms illustrating the effects of small and large $L_s(\dot{i}_1 + \dot{i}_2)$ on the same inverter under identical line and load conditions. Figure 2.12(A) shows the i-v characteristic of the tunnel diode where the effect of $L_s(\dot{i}_1 + \dot{i}_2)$ is small. As a result, $(i_1 - i_2)_b = (i_1 - i_2)_a$ while $(i_1 + i_2)_b \neq (i_1 + i_2)_a$. On the other hand, the effect of $L_s(\dot{i}_1 + \dot{i}_2)$ is large in Fig. 2.12(B), as is evidenced by the facts that $(i_1 \pm i_2)_b = (i_1 \pm i_2)_a$. Also, the path of constant-current switching starts at the peak and the valley when $L_s(\dot{i}_1 + \dot{i}_2)$ is large, as is demonstrated in Fig. 2.12(B).

Figure 2.13(A) and (B) demonstrate the two possibilities where the two diodes will operate on the same voltage segment. In Fig. 2.13(A), diode #2 arrives at the valley and

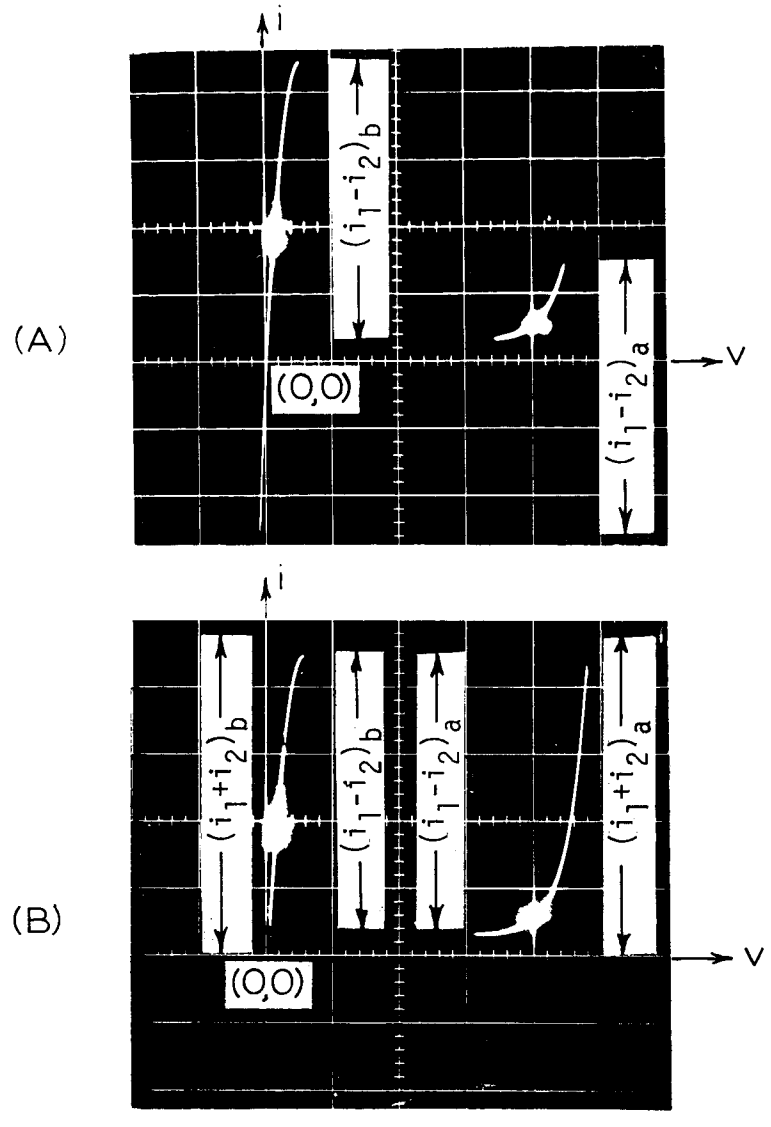


Fig. 2.12. Continuity of $(i_1 - i_2)$ and $(i_1 + i_2)$ Due to L_w and L_s

(A) $L_s = 0$, $R_L = \infty$, $E_i = 225$ mV,
$(i_1 - i_2)_a = (i_1 - i_2)_b = 20$ mA,
$(i_1 + i_2)_a = -5$ mA, $(i_1 + i_2)_b = 25$ mA.

(B) $L_s = 1$ mH, $R_L = \infty$, $E_i = 225$ mV,
$(i_1 - i_2)_a = (i_1 - i_2)_b = 20$ mA,
$(i_1 - i_2)_a = (i_1 + i_2)_b = 25$ mA.

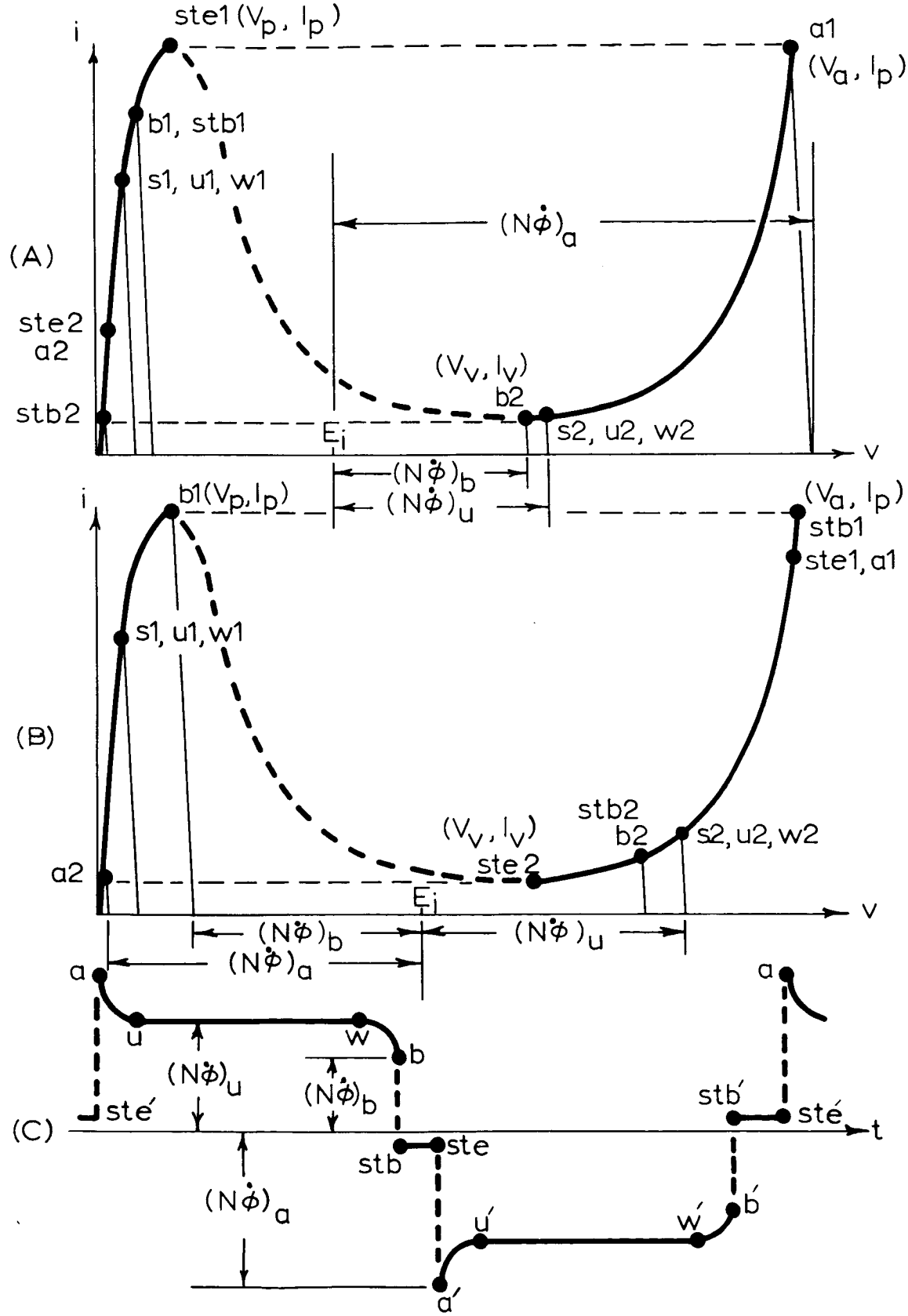


Fig. 2.13. Operation of Both Diodes on (A) Low-Voltage Segment, (B) High-Voltage Segment, and (C) The Corresponding Induced Voltage.

switches before diode #1 reaches the peak, resulting in the operation of both diodes on the low-voltage segment. In Fig. 2.13(B), diode #1 arrives at the peak and switches before diode #2 reaches the valley, resulting in the operation of both diodes on the high-voltage segment. The input voltage E_i of Fig. 2.13(B) is usually larger than that of Fig. 2.13(A). Points s, a, b, and numbers 1 and 2 all have the same meanings as before. Points stb and ste are used to symbolize the beginning and the ending of the small-voltage step. While both Fig. 2.13(A) and (B) can be used to explain the waveform of Fig. 2.13(C), only Fig. 2.13(A) is used here for illustrative purpose. Start with both diodes operating at the singular points s1 and s2, respectively. This corresponds to the constant-voltage plateau between u and w on the induced-voltage waveform of Fig. 2.13(C). After passing w, the saturation of the core causes i_1 to move toward I_p and i_2 to move toward I_v until diode #2 reaches the valley and switches after passing b2. The switching takes place along a constant-current path. The arrival of diode #2 at stb2 marks the beginning of the step interval during which both i_1 and i_2 increase along the low-voltage segment until diode #1 reaches the peak and switches horizontally to a1 while diode #2 stays at a2. Both diodes then proceed toward their respective singular points, thus concluding one half cycle of the inverter operation.

The amplitudes of $(N\dot{\phi})_a$, $(N\dot{\phi})_b$, and $(N\dot{\phi})_u$ when $L_s(\dot{i}_1 + \dot{i}_2)$ is large can be calculated by graphical analyses similar to those described in earlier sections where the effect of $L_s(\dot{i}_1 + \dot{i}_2)$ is small. These analyses are illustrated

in Fig. 2.13(A) and (B). However, the accuracies of these analyses decrease considerably as the effect of $L_s(\dot{i}_1 + \dot{i}_2)$ becomes larger, since these graphical analyses rely heavily on the assumption of zero $L_s(\dot{i}_1 + \dot{i}_2)$.

In the following discussion, a modification in the theoretical approach presented in the earlier sections is used which enables one to calculate the various induced voltages rather accurately regardless of the amount of $L_s(\dot{i}_1 + \dot{i}_2)$. This modification utilizes the property of constant-current switching of the tunnel diodes. Since the constant-current switching must occur alternately at the peak and the valley, the voltage and current conditions of the tunnel diodes immediately before or after the switching of any one diode are known quantities. These quantities are illustrated in Fig. 2.13(A) by points stel and a1 and points b2 and stb2, and in Fig. 2.13(B) by points b1 and stb1 and ste2 and a2. These quantities can then be conveniently utilized to calculate the amplitudes of $(N\dot{\phi})_a$ and $(N\dot{\phi})_b$ regardless of the amount of $L_s(\dot{i}_1 + \dot{i}_2)$. By subtracting equation (2) from equation (1), one obtains:

$$(N\dot{\phi}) = \tfrac{1}{2}\left[(v_2 - v_1) + R(i_2 - i_1)\right] \qquad (26)$$

Notice that the relationship in equation (26) is independent of the amount of $L_s(\dot{i}_1 + \dot{i}_2)$ in equations (1) and (2). Also, the positions of points a and b in Fig. 2.13(A) and (B) are such

that the following approximate relations hold in the case of a properly designed inverter:

$$(v_2 - v_1)_a \approx -V_a \tag{27A}$$

$$(v_2 - v_1)_b \approx V_v \tag{27B}$$

$$R(i_2 - i_1)_a << V_a \text{ or } V_v \tag{27C}$$

$$R(i_2 - i_1)_b << V_a \text{ or } V_v \tag{27D}$$

Consequently, from equations (26) and (27),

$$\left|(N\dot{\phi})_a\right| \approx V_a/2 \tag{28A}$$

$$\left|(N\dot{\phi})_b\right| \approx V_v/2 \tag{28B}$$

for either Fig. 2.13(A) or (B).

With a source inductance of one millihenry, the experimental $(N\dot{\phi})_a$ and $(N\dot{\phi})_b$ for the same line and load conditions as those of Fig. 2.11 (where $L_s = 0$) are shown in Fig. 2.14. They are compared with the theoretical values (listed inside the parentheses) calculated from equation (28), using $V_a = 480$ mV and $V_v = 320$ mV for the particular tunnel diodes used in the test circuit. The small differences between the corresponding theoretical and experimental values are attributed to the inaccuracies of the approximate relations of equations (27) and (28).

The induced voltage $(N\dot{\phi})_u$ and the associated time interval T_{uw} are not calculated as they are identical to the corresponding ones in Fig. 2.11. The mere addition of the source inductance in the case of Fig. 2.14 does not change the singular-point operations of Fig. 2.11, as both $\dot{i}_1$ and $\dot{i}_2$ are zero during singular-point operations.

The time intervals associated with the spikes and the curvatures of Fig. 2.14 are calculated from equations (18) and (24) using the values given in equation (28). Results obtained are listed in the parentheses, and are in good agreement with the corresponding time intervals observed:

For Fig. 2.14(A), $T_{au} + T_{wb} = 1.8$ ms (1.83 ms)

For Fig. 2.14(B), $T_{au} + T_{wb} = 1.6$ ms (1.83 ms)

For Fig. 2.14(C), $T_{au} + T_{wb} = 1.6$ ms (1.83 ms)

In the oscillograms of Fig. 2.14, a short step interval can be seen at the beginning of each half cycle. The amplitudes

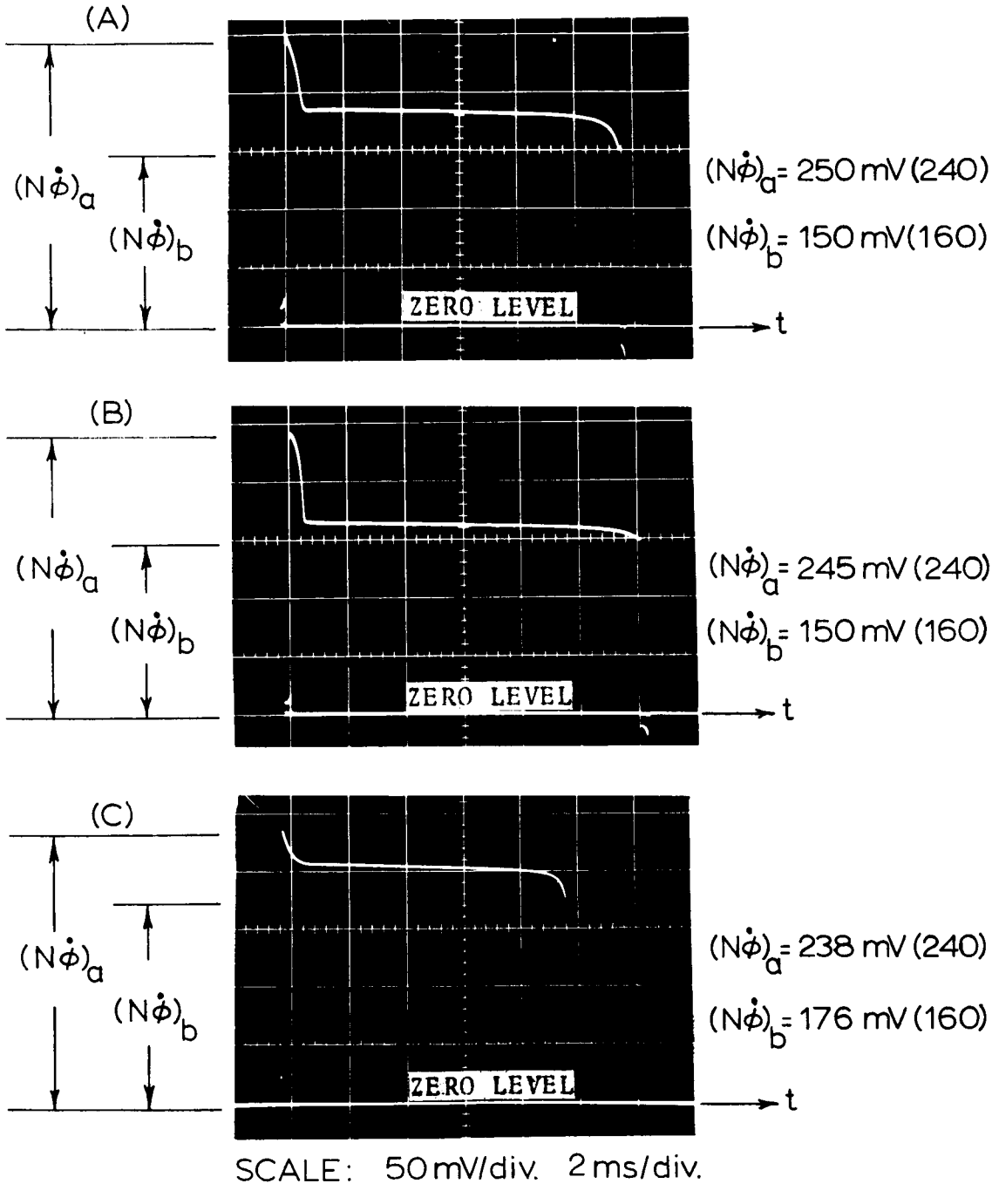


Fig. 2.14. Oscillogram of Induced-Voltage Waveform, L_s=10 mH.

(A) E_i = 200 mV, R_L = ∞ , L_s = 1 mH

(B) E_i = 180 mV, R_L = 110 ohms, L_s = 1 mH

(C) E_i = 280 mV, R_L = 40 ohms, L_s = 1 mH

of the induced voltages during the steps are very small. These small voltages are readily explained in terms of equation (26), with the difference between v_2 and v_1 now small due to the operation of both diodes on the same segment of their respective characteristics. The time intervals for the voltage steps are treated in the next section.

Steps of Induced Voltage

From the discussions in the previous sections, it is understood that steps of small induced voltages occur during the intervals when the large $L_s(\dot{i}_1 + \dot{i}_2)$ cause both diodes to stay on the same positive-resistance segment. The step intervals end when either the peak or the valley of any one diode is reached. Also, due to the continuities required for the source current $i_1 + i_2$ (demanded by L_s) and for the difference in current $i_1 - i_2$ (demanded by L_w), the diode current is constant at I_p or I_v as it switches across its negative-resistance region. With the physical nature of the step phenomena now understood, formulas will be derived for the calculations of the time intervals associated with the steps. The analysis is carried out by assuming ideal N-shaped characteristics for the diodes shown in Fig. 2.7(B), i.e., $v = ir$ and $v = V + ir$ for the low- and high-voltage segment, respectively. Also, in light of the experimental i-v characteristic of the tunnel diodes shown in Fig. 2.3 where $i_2 \approx I_v$ between $v = V_v$ and $v = V_h$, $\dot{i}_2$ is assumed to be zero after point (V_h, I_v) is reached.

Consider first the conditions demonstrated in Fig. 2.15(A) where diode #2 arrives at the valley and switches before diode #1 reaches the peak. Both diodes then operate on the low-voltage segment, with $v_1 = i_1 r$ and $v_2 = i_2 r$. Inserting equation (26) into equation (1) with v_1 and v_2 replaced by $i_1 r$ and $i_2 r$ respectively.

$$E_i = L_s(\dot{i}_1 + \dot{i}_2) + \tfrac{1}{2}(r + R + 2R_s)(i_1 + i_2) \qquad (29)$$

From Fig. 2.15(A), P is the difference and $2I_v + P$ is the sum of i_1 and i_2 at the beginning of the step interval at which $i_1 = I_v + P$ and $i_2 = I_v$. Use $2I_v + P$ as the initial condition for $i_1 + i_2$ and solve equation (29) for $(i_1 + i_2)$. This gives

$$i_1 + i_2 = \frac{2E_i}{r + R + 2R_s} + (2I_v + P - \frac{2E_i}{r + R + 2R_s})\exp(\frac{r + R + 2R_s}{2L_s})t \qquad (30)$$

From equation (26), voltage $N\dot{\phi}$ is small during the step interval as both diodes are operating on the low-voltage segment which permits only a small difference between v_1 and v_2. The small induced voltage causes negligible load current i_L, and the equation for the saturated core characteristic becomes:

$$N\phi \approx N\phi_s + L_w(i_1 - i_2) \qquad (31)$$

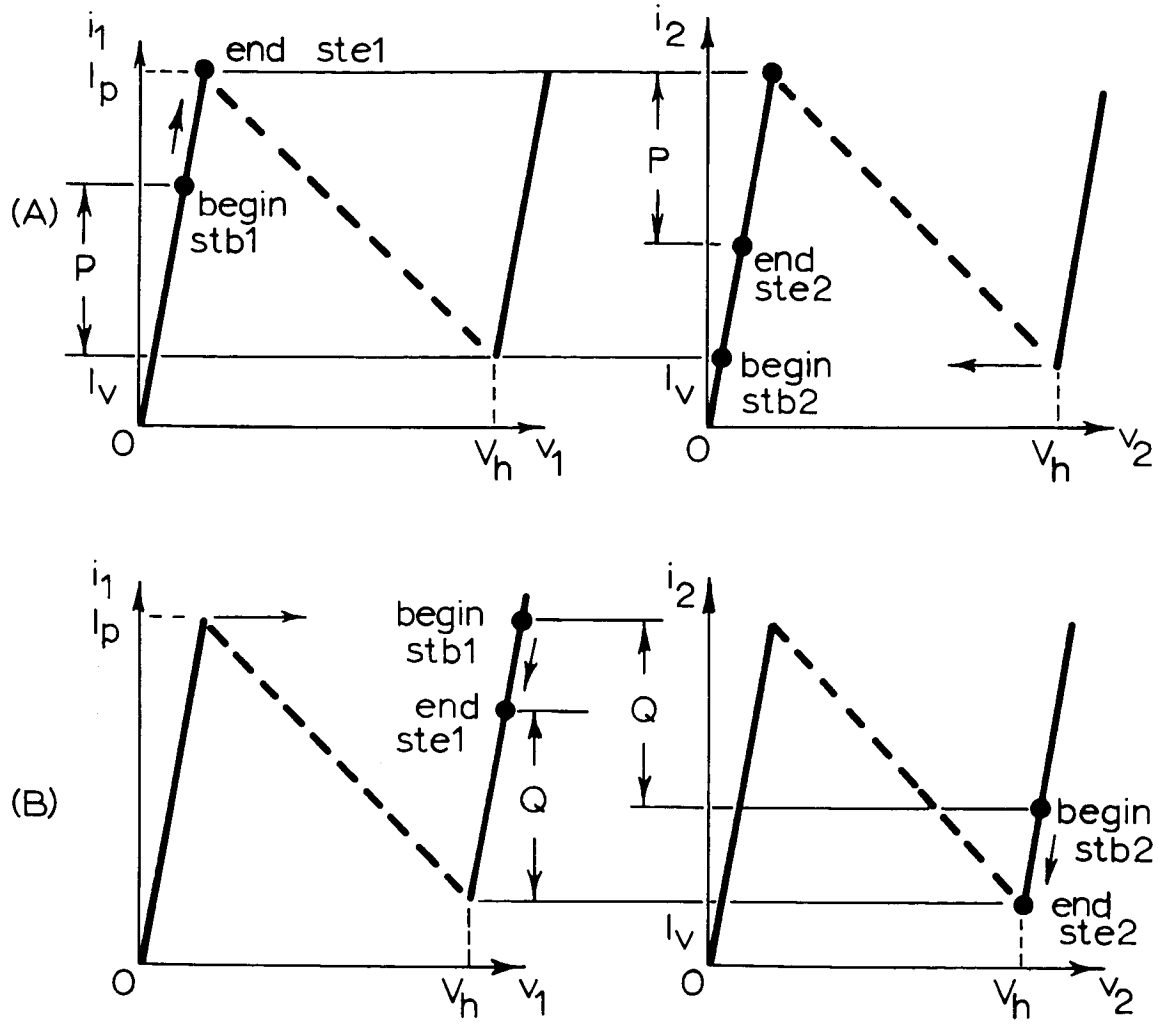


Fig. 2.15. Operating Characteristics of the Tunnel Diodes during Step Interval.

(A) Both Diodes Operate on the Low-Voltage Segment

(B) Both Diodes Operate on the High-Voltage Segment

Differentiation of equation (31) reveals that a small $\dot{N\phi}$ results in a small $(\dot{i}_1 - \dot{i}_2)$. Consequently, during the step interval the two diode currents increase at almost an identical rate along the low-voltage positive-resistance segment, maintaining approximately the same difference P between i_1 and i_2 throughout the step interval. When the step interval ends at $i_1 = I_p$, the sum of i_1 and i_2 approaches $2I_p - P$, as can be seen from Fig. 2.15(A). Substituting this boundary condition into equation (30) and solve for the variable t, the step interval T_{step} becomes:

$$T_{step} = \frac{2L_s}{r + R + 2R_s} \ln \frac{2E_i - (2I_v + P)(r + R + 2R_s)}{2E_i - (2I_p - P)(r + R + 2R_s)} \qquad (32)$$

In order to find the initial current difference P, differentiate equation (31) and substitute it into equation (26),

$$\dot{i}_1 = (1/2L_w) \bullet (v_2 - v_1 + i_2R - i_1R) + \dot{i}_2 \qquad (33)$$

At the beginning of the step when diode #2 just arrives at the point (V_h, I_v) and switches, the conditions of the diodes are that $v_1 = i_1r$, $v_2 = V_h$, $i_2 \approx I_v$, and $\dot{i}_2 \approx 0$ as explained at the beginning of this section. Upon substituting these conditions first into equation (33) and then into equation (2), and

remembering that $P = i_l - I_v$ at the instant of switching, the initial current difference P becomes:

$$P = \frac{L_w(2E_i - V_h - I_vR - 2I_vR_s) - L_s(V_h + I_vR)}{L_w(r + R + 2R_s) - L_s(r + R)} - I_v \qquad (34)$$

Normally, $L_w >> L_s$, and equation (34) reduces to

$$P = \frac{(2E_i - V_h) - I_v(r + 2R + 4R_s)}{r + R + 2R_s} \qquad (35)$$

The combination of equations (32) and (35) yields

$$T_{step} = \frac{2L_s}{r + R + 2R_s} \ln \frac{V_h - I_v r}{4E_i - V_h - 2I_p(r + R + 2R_s) - I_v(r + 2R + 4R_s)} \qquad (36)$$

It is noted that equations (35) and (36) are derived under the assumption that both diodes are operating on the low-voltage segment of their respective characteristics, as illustrated in Fig. 2.15(A). However, steps of small induced voltage can also be caused by operating both diodes on their respective high-voltage segments, as illustrated in Fig. 2.15(B). When this happens, similar techniques employed in deriving equations (35) and (36) yield the following results:

$$Q = \frac{(-2E_i + V_h) + 2I_p(r + R + 2R_s) - I_v r}{r + R + 2R_s} \tag{37}$$

$$T_{step} = \frac{2L_s}{r + R + 2R_s} \ln \frac{V_h - I_v r}{-4E_i + 3V_h + 2I_p(r + R + 2R_s) + I_v(-r + 2R + 4R_s)} \tag{38}$$

where Q is the initial difference between i_1 and i_2 at the beginning of the step interval when both diodes are operating on the high-voltage segment.

Fig. 2.16 shows an oscillogram of induced voltages under conditions of different source inductances and input voltages. The top trace is the induced voltage without source inductance, and therefore, without a step. The middle trace demonstrates steps caused by the operation of both diodes in the low-voltage segment, while the bottom trace shows the steps caused by the operation of both diodes in the high-voltage segment. Using equations (36) and (38), the step intervals in Fig. 2.16(B) and (C) are calculated to be 1.3 and 1.7 milliseconds respectively. These compare favorably with the measured value of approximately 1.5 milliseconds for each. Figure 2.17 shows in dotted lines the experimental results of L_s vs. T_{step} where the steps are caused by both diodes operating on the low-voltage segment. These data are in good agreement with those calculated from equation (36). Equally good agree-

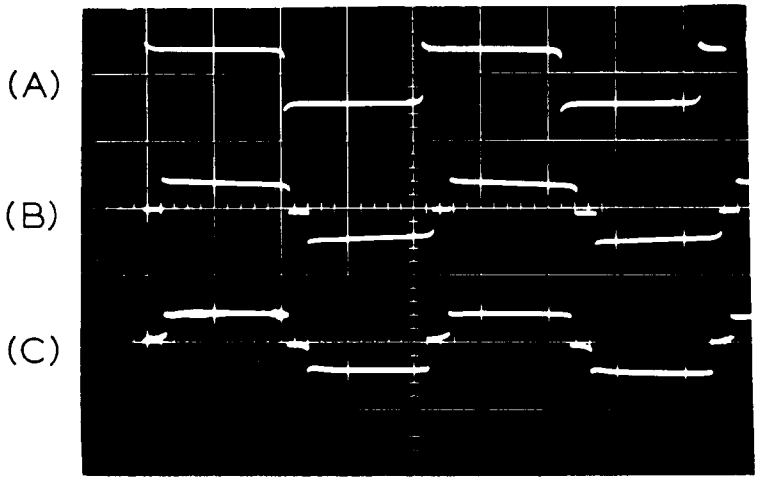


Fig. 2.16. Oscillograms of Induced Voltages with Small-Voltage Steps.

(A) E_i = 240 mV, R_s = 0, L_s = 0, $R_L = \infty$
(B) E_i = 240 mV, R_s = 1 ohm, L_s = 10 mH, $R_L = \infty$
(C) E_i = 310 mV, R_s = 1 ohm, L_s = 10 mH, $R_L = \infty$

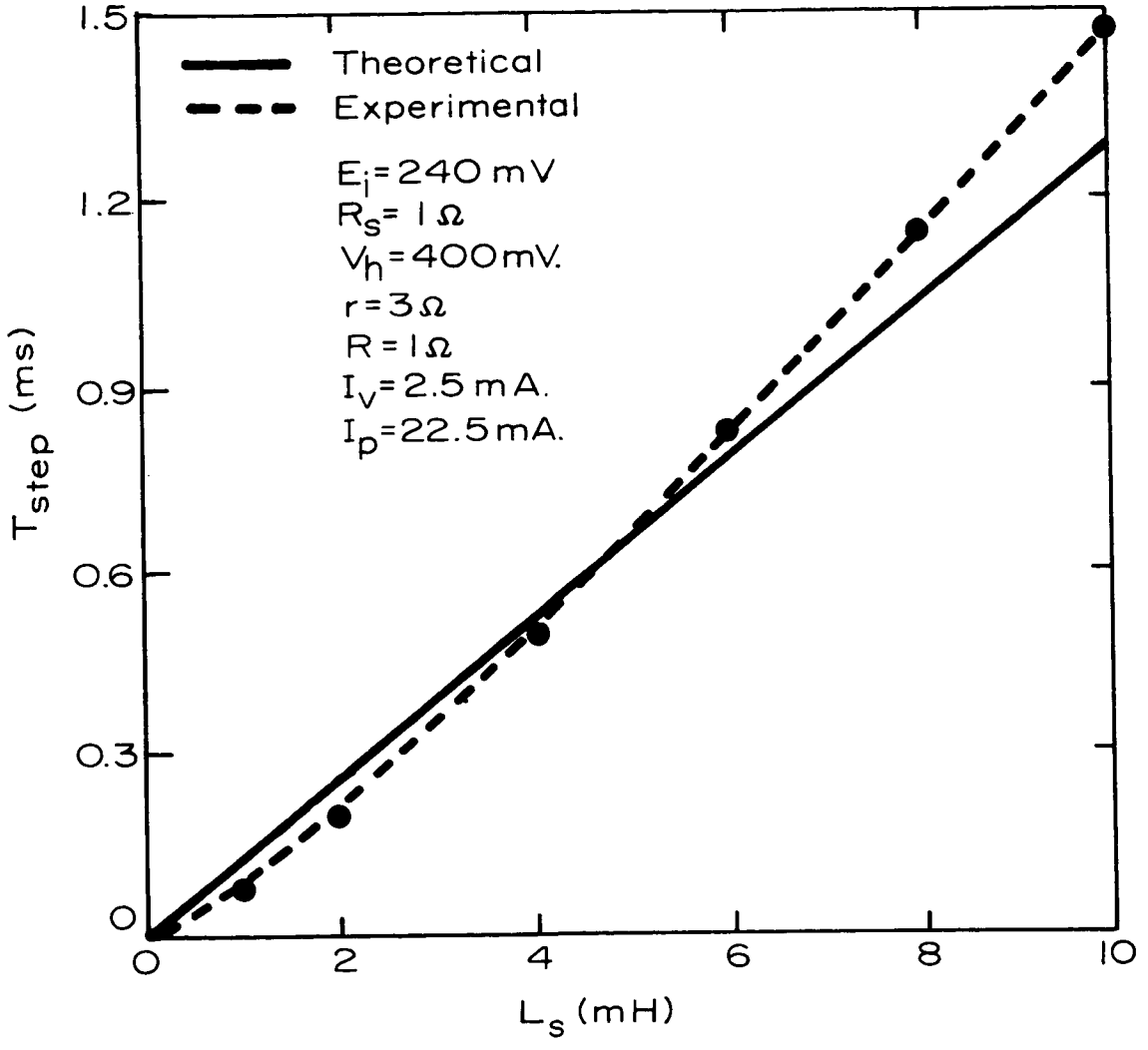


Fig. 2.17. Step Interval vs. Source Inductance with Both Diodes Operating on the Low-Voltage Segment.

ments exist between the experimental results and equation (38) when both diodes operate on the high-voltage segment. These data are illustrated in Fig. 2.18.

Due to the high input current and the low output voltage during the step, the efficiency of the inverter suffers considerably. From equations (36) and (38), the step interval is directly proportional to the amount of source inductance that exists inadvertently in the source supplying E_i. In equation (36) which applies to the operations of both diodes on the low-voltage segment, the step interval diminishes with an increase in E_i. On the other hand, the step interval increases with an increase in E_i when both diodes are operating on the high-voltage segment, as is evident from equation (38). Also, the step intervals increase with the peak currents of the tunnel diodes used in the inverter. This is numerically illustrated in Appendix B. Due to the fact that the existence of certain amount of L_s in the source is inevitable, and that the steps of small induced voltage caused by this L_s reduce drastically the inverter efficiency, one cannot but cast a dim prospect on the future of the high-current Marzolf inverters for power applications.

It is interesting to note that if two straight, round conductors each with a radius of two centimeters and a length of one meter are placed ten centimeters apart along the same axis, then the inductance of this two-wire transmission line is approximately $(0.1)(1 + \ln 5)$ microhenries, i.e., 0.75 microhenries. [14] If such transmission lines were used to supply power from a source to an inverter employing tunnel

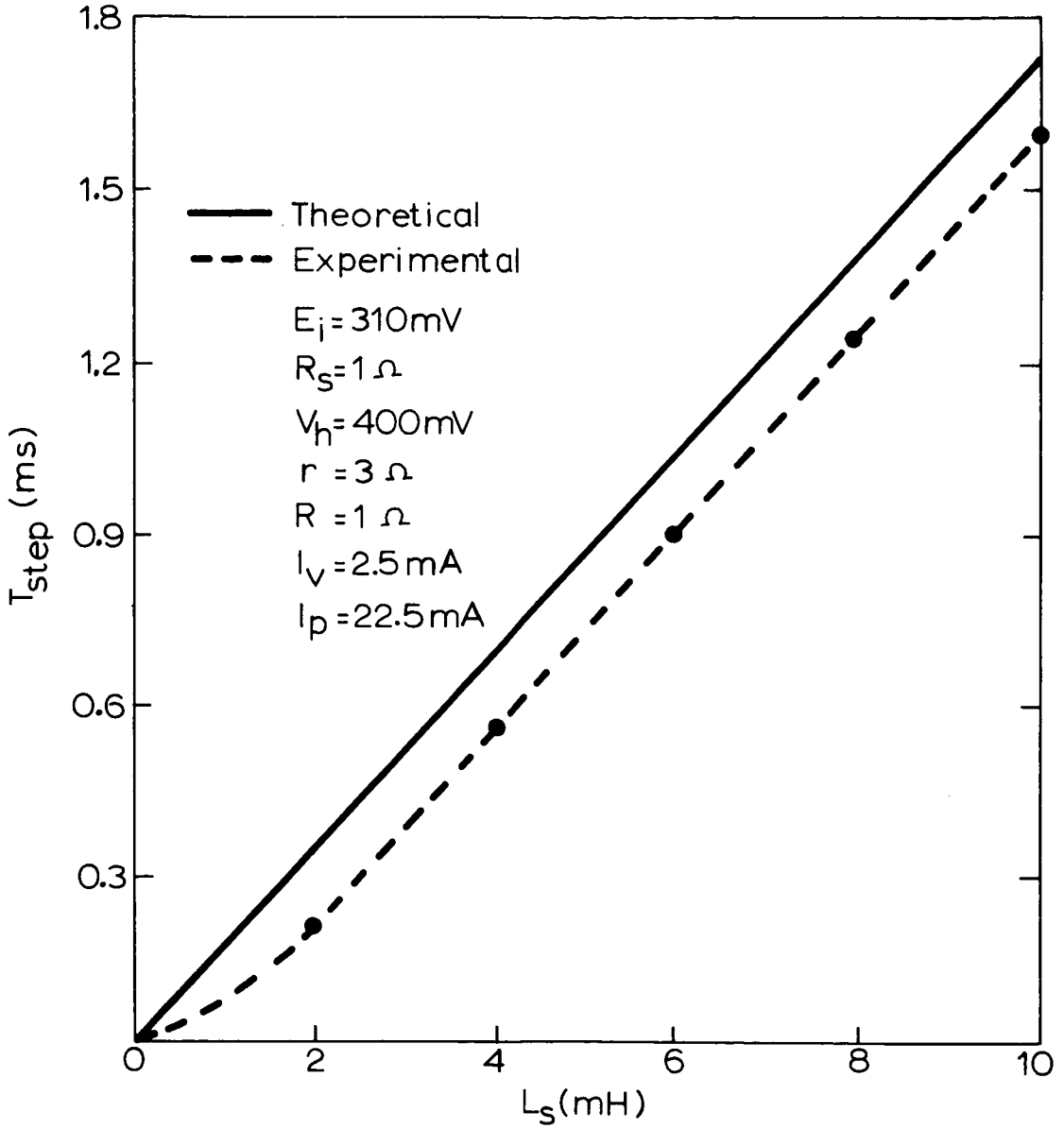


Fig. 2.18. Step Interval vs. Source Inductance with Both Diodes Operating on the High-Voltage Segment.

diodes whose peak currents are one hundred amperes, a step interval in the order of 0.4 milliseconds would result, as illustrated in Appendix B. Step intervals of the same order of magnitudes have been reported in the literature for a 100-ampere Marzolf inverter in which the transmission lines from the source to the inverter appeared to bear some resemblance to the two-wire system described in this paragraph.[9]

Future Research on Marzolf Inverter

There are many problems left to be solved for the Marzolf inverter. For instance, no analysis of the inverter with a non-unity power-factor load appears to have been documented in the literature. The effects of leakage inductances and winding capacitances to the operation of the inverter are other topics of interest. The analysis of the starting mechanism of the inverter in terms of a phase plane approach is another promising topic in the field of nonlinear analysis. Further work in these areas would surely be both challenging and rewarding.

Conclusion

In this chapter, a combined graphical and analytical technique is successfully employed to solve the steady-state performances of the Marzolf inverter. The analysis explains physically the occurrence of the steps and calculates them rather accurately. The technique also explains and mathemati-

CHAPTER III

DC TO DC CONVERTER CONTROLLED BY A MAGNETICALLY-COUPLED MULTIVIBRATOR WITH ASYMMETRIAL OUTPUT*

Although the Marzolf inverter analyzed in Chapter II provides a simple and reliable means for voltage step-up, the efficiency of the inverter is quite low due to the inherent voltage-current characteristics of the tunnel diodes. For better inversion efficiency, other switching elements such as transistors and controlled rectifiers are used in other types of magnetically-coupled inverters. Since it is only in the rare case of voltage step-down where dc to dc conversion is accomplished by simply dropping the voltage through a dissipative element, transformation of dc voltage levels invariably involves at least one inversion process.[16] The transistor or SCR inverter circuits thus become essential for more efficient dc to dc power conversion systems. In these circuits the semiconductor switches are either fully on or off during each cycle of operation. Their capabilities of blocking the forward voltage when they are fully off are much better than those of the

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*The material contained in this chapter is taken almost exclusively from a paper which the author was the major contributor. The paper is listed as reference (15) of this dissertation.

cally determines the different amplitudes and time intervals associated with the voltage spikes and curvatures for different line and load conditions. The effects of source inductances on the spikes and curvatures are also included in the discussion. The spikes and curvatures of the induced voltages are related to the inherent nonlinear tunnel diode characteristics and the current continuities required by the saturated core and/or the source inductance. The steps of small induced voltages are found to be caused primarily by the source inductance, which is the combined inductances of the source and the transmission lines between the source and the inverter.

By extending the same technique to the analysis of other types of magnetically-coupled multivibrators such as the Royer circuit,[4] it is hoped that the phenomena of voltage spikes and curvatures of such multivibrators can be more thoroughly understood.

tunnel diodes. In order to utilize efficiently the inherent i-v characteristics associated with these switching devices of superior blocking capabilities, dc input voltages to transistor or SCR inverters are normally much higher than those of the tunnel diode inverters.

The higher dc voltages call for the series connections of as many low-voltage sources as practical. Due to the changing environmental conditions and load demands, the output voltage of each low-voltage dc source, and therefore the sum of the series-connected voltages, are not constant. However, regulated dc voltages are often desirable for space applications. Regulated dc to dc converters therefore become an important part of the spacecraft power-conditioning systems.

There are many different ways through which a variable dc voltage can be changed into one with constant amplitude. The simplest type of dc regulator is the series regulator shown schematically in Fig. 3.1(A). Here, the impedance of the transistor between the fluctuating input voltage E_i and output voltage E_o is controlled to vary in such a way as to keep E_o constant. The equivalent circuit of Fig. 3.1(A) is shown in Fig. 3.1(B). As is evident from Fig. 3.1(B), the maximum possible efficiency for this regulator is E_o/E_i. Since the input voltages for space power-conditioning systems (for instance, the output voltages from the solar cells) normally vary over a rather wide range, this method of regulation is not practical for space power applications and is often referred to as dissipative regulation.

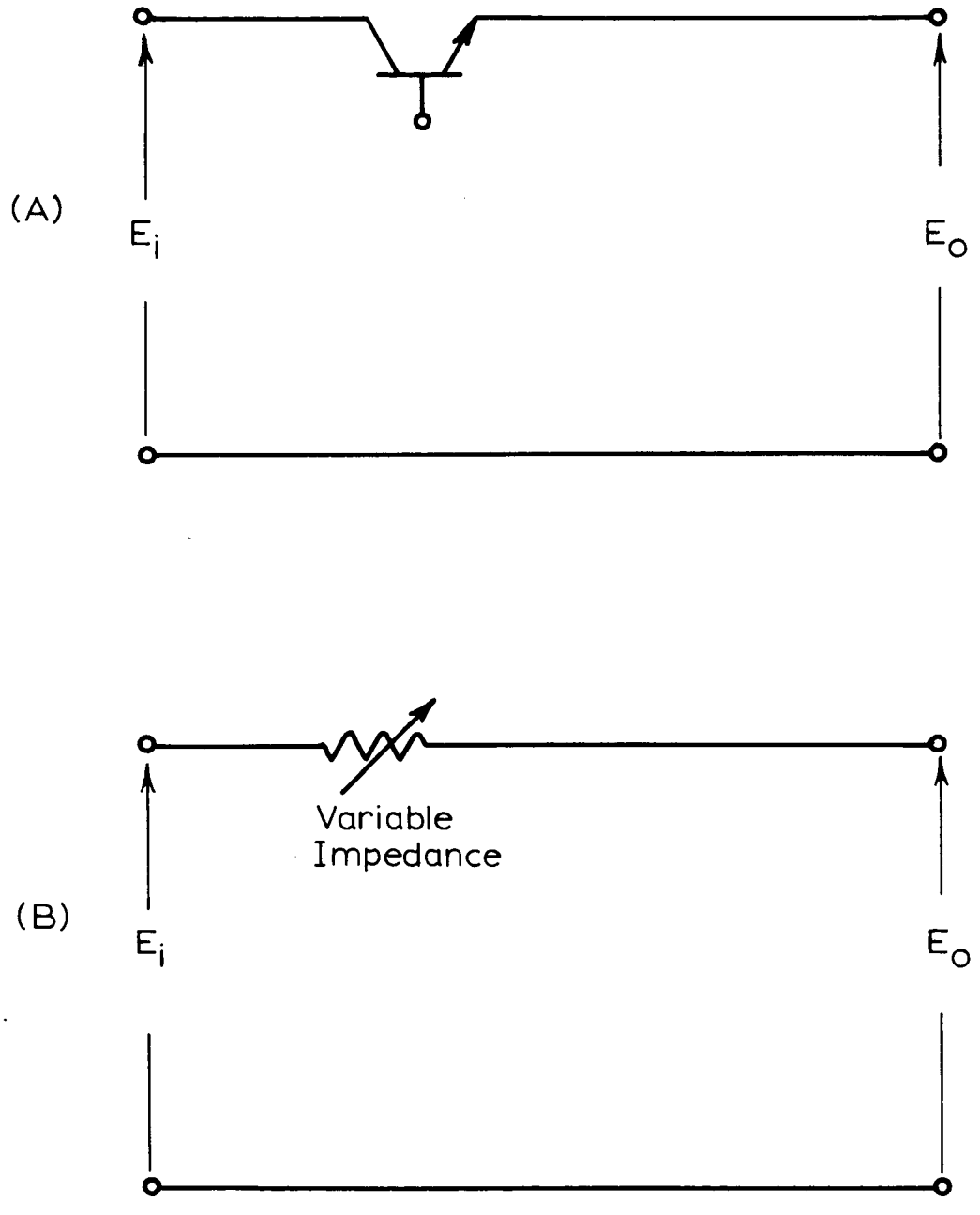

Fig. 3.1. Series Regulator.

(A) Schematic Diagram

(B) Equivalent Circuit

For better efficiencies, the regulation has to be achieved through nondissipative means. The main semiconductors in these nondissipatively regulated dc to dc converters are switched either fully on (with small voltage drops across them) or fully off (with essentially no current through them) in a controlled fashion. Fig. 3.2 shows the schematic diagram of a typical example of one such converter.[17] The LC filter reduces the output-voltage ripple caused by the switching of the transistor. The diode provides a path for the inductor current during the off time of the transistor. While the efficiency of the circuit in Fig. 3.2 is generally higher than that of Fig. 3.1, the output voltage E_o in either case is restricted to an amplitude less than E_i.

Dc to dc converters using cyclic inductive-energy storage and release as the means for voltage transformation, often called flyback circuits,[18] remove this restriction by providing an $E_o \geq E_i$. The schematic diagram of the flyback circuit is shown in Fig. 3.3. Regulation is achieved by causing the transistor to have variable on time and constant off time, or variable off time and constant on time,[19,20,21] or both variable on time and variable off time.[15] Not only is this type of regulated converter very efficient, as input power is handled only once in the inverter stage, but it also minimizes the number of components used and still accomplished the desired voltage step-up. The operation of the basic flyback circuit is described in some detail at a later section of this chapter.

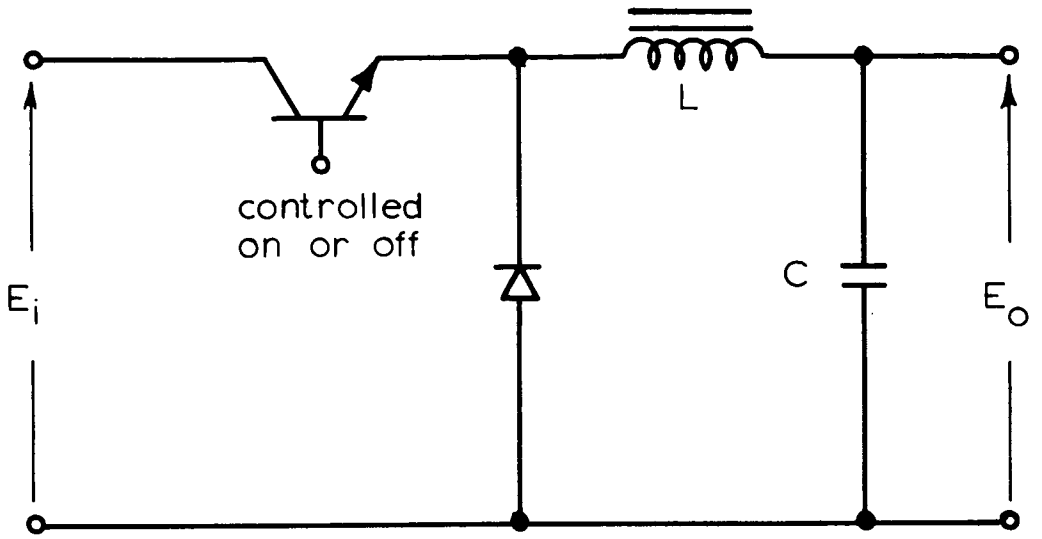

Fig. 3.2. Schematic Diagram of the Series Switching Regulator.

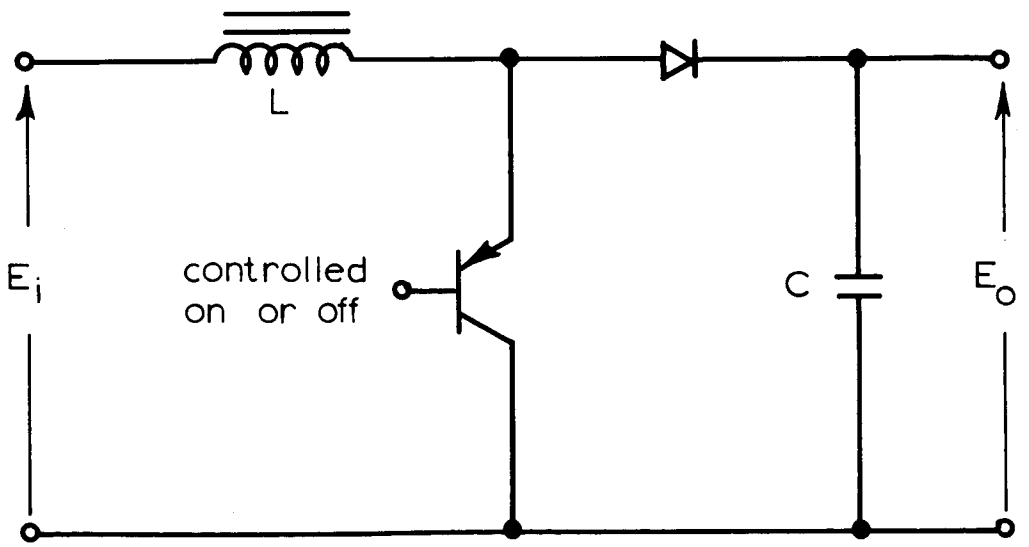

Fig. 3.3. Schematic Diagram of the Basic Flyback Circuit.

In both SCR and transistor types of switching-mode regulators and in transistor dc to dc converters such as Fig. 3.3, it frequently has been found desirable to employ one or more square-loop cores as timing elements for controlling the duty cycle of the power switching transistors. Quite often the designer of such a circuit is led by his desire for high efficiency and a low degree of complexity to a system of duty-cycle control which is characterized by a constant on time and a controllable off time.[22] Such constant-on-time systems are not without certain disadvantages, however, particularly when the converter in which they are employed is to be operated over a wide range of input voltage and output load.

In designing any high-performance switching-mode regulation system, one of the most commonly encountered problems is that of assuring stable operation under all specified working conditions and at the same time achieving small size, low weight, high efficiency, good regulation, fast response, and small output ripple. Usually, these factors may be traded one for the other, and as a consequence, compromises must be made to obtain the best overall performance. The degree of difficulty in making these compromises is directly related to the range of frequencies over which the dc to ac inversion takes place. For instance, it is generally more difficult to maintain a relatively constant loop gain as the frequency range over which the closed-loop system operates becomes wider. A small range is therefore desirable in establishing the proper optimization between the system stability and the transient response. Also,

the smaller the range in frequency variation, the easier it usually is to keep the output ripple small without using heavier and more bulky filter components. Additionally, a smaller frequency range permits more optimum design between converter size and weight and its associated losses. For these reasons, a circuit which controls the duty cycle and which operates at a constant frequency would seem to be the best choice for good overall performance. However, as additional circuitry is required to fix the frequency, a duty-cycle regulated converter that operates at a constant frequency generally is more complex than one with variable frequency.

This chapter describes a nondissipatively regulated variable-frequency dc to dc converter with variable on time and variable off time, utilizing the basic circuit of Fig. 3.3. The converter is physically very simple but nevertheless exhibits high performance characteristics that are normally found only in more complicated circuits. Compared with other variable-frequency converters which either have constant on time or constant off time, the frequency range of this converter is smaller over a wider range of load conditions, specifically, from full load down to rather light load. As the load approaches that of an open circuit, this converter enters into a high-frequency mode of operation rather than achieving the required low duty cycle by operating at a very low frequency. This high-frequency operation enables the output-voltage ripple to remain small. To make possible the combination of high performance and simplicity, an unconventional magnetic-semiconductor voltage-

to-duty-cycle encoder is used as a basic part of the closed-loop regulation system to control both the on time and the off time of the main power transistor.

The converter employs a voltage-feedback arrangement for the base drive of the main switching transistor which takes full advantage of the variable-on-time variable-off-time feature of the voltage-to-duty-cycle encoder. The loss associated with the base circuit during the on time of the power transistor is kept within reasonable limits, since the on-time interval during which this loss occurs decreases with either an increase in the input voltage or a decrease in the output load. With this loss thus limited, high efficiencies over a wide range of input voltage and output load are achieved.

In this chapter, the converter circuit will be described first, followed by its theory of operation. The converter enters into three different modes of operation over the entire regulation range. These three modes are analyzed and explained in detail. A comparison of operating frequencies between this converter and other variable-frequency converters is given next. Finally, the performance characteristics of a test circuit are shown.

Circuit Description

The complete schematic diagram of the converter is shown in Fig. 3.4. The actual circuit components are listed in Table II. In the following discussion, the circuit is divided into

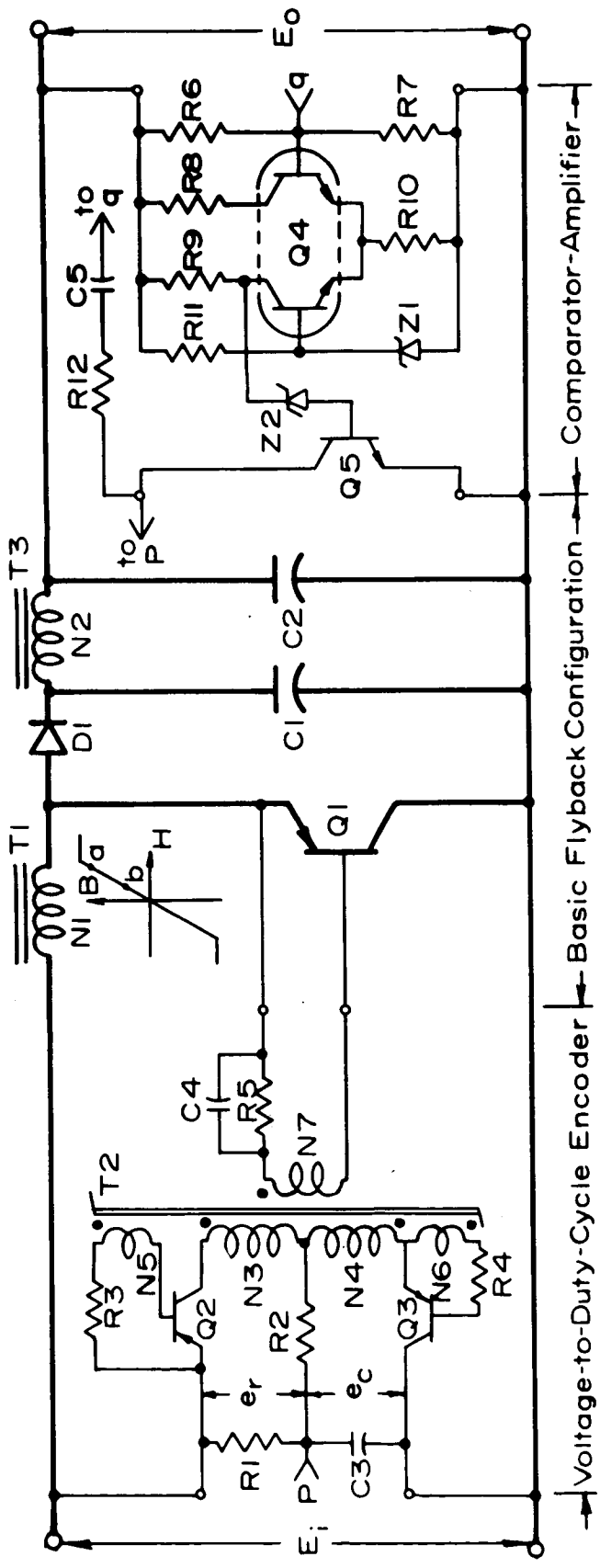

Fig. 3.4. Complete Regulated Dc to Dc Converter.

TABLE II

Actual Components of Fig. 3.4

C1, C2	: 160 μF		R2	: 39	Ω
C3	: 1 μF		R3	: 1.62	kΩ
C4	: 0.047 μF		R4	: 150	Ω
C5	: 0.47 μF		R5	: 22	Ω
D1	: Westinghouse 2N3880		R6	: 22	kΩ
N1	: 110 turns, #16 AWG		R7, R12	: 6.8	kΩ
N2	: 180 turns, #24 AWG		R8, R9	: 10	kΩ
N3, N4	: 450 turns, #34 AWG		R10	: 4.7	kΩ
N5, N6, N7	: 90 turns, #34 AWG		R11	: 39	kΩ
Q1	: T.I. 2N1907		T1	: Magnetics, Inc. 55324-L6	
Q2, Q3	: G.E. 2N1926		T2	: Magnetics, Inc. 80034-¼D	
Q4	: G.E. 2N2641		T3	: Magnetics, Inc. 55204-A2	
Q5	: G.E. 2N2909		Z1	: G.E. 1N1768	
R1	: 33 kΩ		Z2	: G.E. 1N1776	

three major parts - the basic flyback configuration, the voltage-to-duty-cycle encoder, and the comparator-amplifier.

Basic Flyback Configuration

The basic flyback configuration shown earlier in Fig. 3.3 is used in Fig. 3.4 to provide a step-up in voltage from the input E_i to the output E_o. In addition to the filter capacitor C1, the LC filter consisting of capacitor C2 and a small choke with winding N2 is employed to further reduce the output ripple of E_o. Core T1 of the basic flyback configuration has a linear flux density B versus field intensity H characteristic such as that shown in the diagram. This core, with its single winding N1, will be referred to hereafter as the energy-storage reactor.

The operation of this circuit has been described in the literature, and therefore is reviewed here only briefly. Power transistor Q1 is cyclically switched on and off by the output of the voltage-to-duty-cycle encoder. During the on time of Q1, diode D1 is reverse-biased by E_o, and load current is supplied by the output filter capacitors C1 and C2. Meanwhile, E_i is impressed across N1, causing the current in the winding and the flux density in the energy-storage reactor to increase, say, from point b to point a. When Q1 is turned off, continuity of current through N1 is maintained through diode D1, the output filter, and the load. The polarity of the induced voltage across N1 is reversed, causing the flux density to decrease from a to b during the off-time interval of Q1.

Voltage-To-Duty-Cycle Encoder

The voltage-to-duty-cycle encoder involves an asymmetrical magnetically-coupled multivibrator which provides the base drive to the main switching transistor Q1. The semiconductor and magnetic elements of the multivibrator are transistors Q2, Q3 and core T2. Core T2 has a square-loop B versus H characteristic, and its physical size is small compared to that of the energy-storage reactor. Dc voltage supplying power to the two halves of the multivibrator are obtained by dividing the input voltage E_i into two components e_r and e_c. The division of voltage is controlled by the impedance of control transistor Q5 of the comparator-amplifier which is in parallel with capacitor C3. The output voltage of the multivibrator appearing across N7 turns on and off the switching transistor Q1 through the current-limiting resistor R5 and the speed-up capacitor C4. When Q2 conducts, Q1 is turned on and voltage e_r across N3 determines the on time. When Q3 conducts, Q1 is turned off, and voltage e_c across N4 determines the off time. By signals fed back from the comparator-amplifier portion of the circuit, the ratio of e_r to e_c is controlled over a very wide range in order to maintain regulation. Resistance R2 is used to prevent C3 from charging and discharging excessively upon saturation of the square-loop core T2; thus, the voltage e_c has lower ripple and is more adequate for control purposes. Despite lack of complexity, this asymmetrical multivibrator serves as a highly effective encoder to control the duty cycle of the power transistor in the basic flyback circuit.

Comparator-Amplifier

As shown in Fig. 3.4, this portion of the converter includes the differential amplifier Q4, the reference zener diode Z1, the output voltage divider R6-R7, and the control transistor Q5. A sample of output voltage appearing at point q is compared to the reference voltage established by Z1. The error is amplified by Q4 before being applied to Q5 which in turn controls voltage e_c directly, and indirectly controls voltage e_r, since $e_r = E_i - e_c$. By so doing, both the on time and the off time are controlled to maintain a constant output voltage E_o. The simple RC lead network of R12-C5 between points p and q of the circuit provides for stable operation of the converter throughout its specified operating range.

Theory of Operation

Depending on the line and load conditions, there are three distinct modes of operation within the regulation range of this converter. After establishing the general mathematical relationships that are central to the operation of the converter, each of the three modes is described, with some of the more detailed aspects being reserved for discussion in the appendices C and D of this dissertation. Throughout the mathematical analysis, the assumption of ideal components with negligible voltage drops across them is made.

An idealized linear B-H characteristic of T1 is shown in Fig. 3.5. An illustrative set of upper and lower boundaries

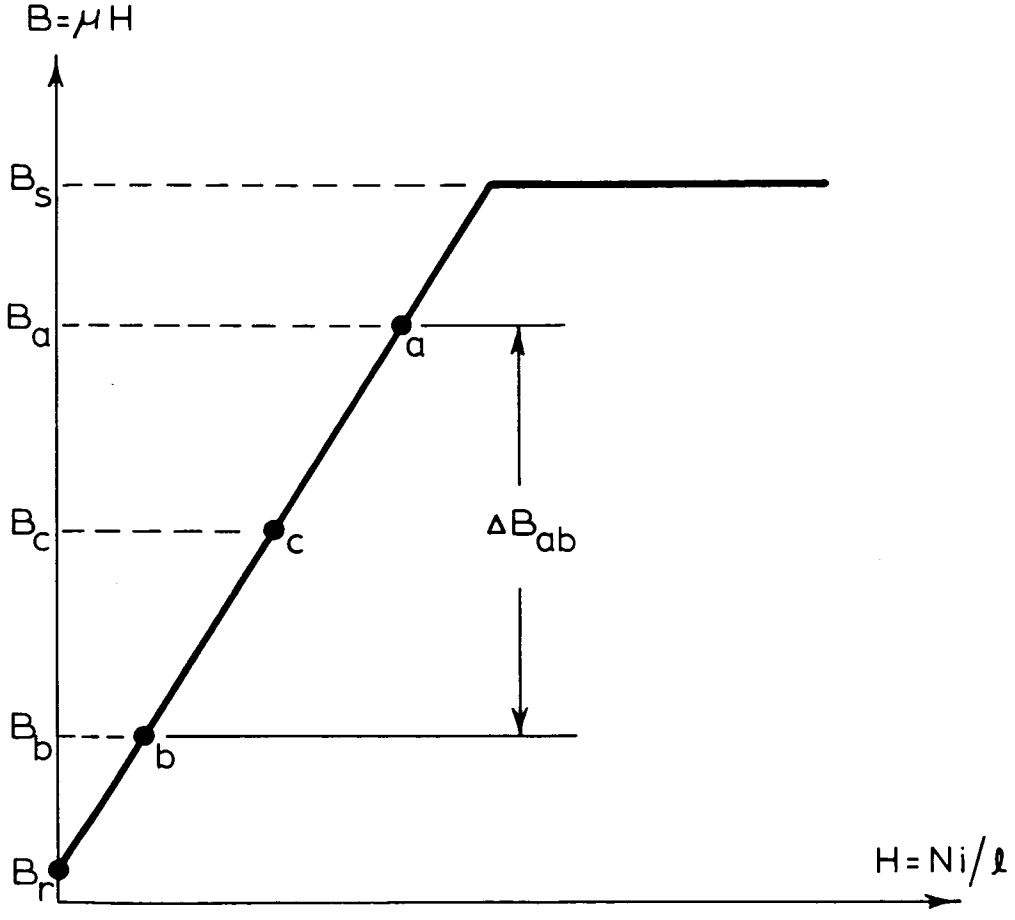

Fig. 3.5. Idealized Linear B-H Characteristic.

of the flux-density levels during one cycle of steady-state operation is represented by B_a and B_b. The following quantities, all in MKS units, are defined:

t_{on} = the time interval during which the power switching transistor Q1 conducts and the flux density of T1 increases in the direction of the saturation level B_s

t_{off}' = that part of the off time of Q1 during which the flux density of T1 decreases in the direction of residual level B_r

t_{off}'' = the remaining portion of the off time of Q1 after the residual level B_r has first been reached

P_o = output power of the converter

η = efficiency of the converter

A, ℓ, N, μ = effective area, mean length of magnetic path, number of turns, and permeability of the energy-storage reactor

I_b, I_c = current through reactor winding N1 corresponding respectively to point b and point c

D = volt-second capacity of square-loop core T2, i.e. the product of N3 and twice the saturation flux of T2

The upward and downward flux-density excursions during the on and off times of the power transistor represent respectively energy stored in and energy released from the linear reactor. For steady-state operation to exist, it is obvious that these two excursions within one cycle of operation must be equal. They are symbolized by ΔB_{ab}, where

$$\Delta B_{ab} = E_i t_{on} / NA = (E_o - E_i) t_{off}' / NA \qquad (39)$$

The flux density level B_c, at the center of the minor loop a-b-a, is represented by

$$B_c = \left(\frac{\mu N}{\ell}\right)\left(\frac{P_o}{E_i \eta}\right)\left[\frac{t_{on} + t_{off}' + t_{off}''}{t_{on} + t_{off}'}\right] \qquad (40)$$

From equations (39) and (40), it is apparent that the minor loop of height ΔB_{ab} migrates up and down the B-H characteristic with variations in line and load conditions. While the maximum flux density B_a, which is $B_c + (\Delta B_{ab}/2)$, is designed always to be lower than the saturation level B_s to avoid a heavy current surge during t_{on}, the minimum flux density B_b can, and sometimes does, dwell at the residual level B_r. The four general equations concerning the operation of this converter are:

$$E_i t_{on} = (E_o - E_i) t_{off}' \tag{41}$$

$$e_r t_{on} = (E_i - e_c) t_{on} = D \tag{42}$$

$$e_c (t_{off}' + t_{off}'') = D \tag{43}$$

$$I_b = I_c - (\Delta I_{ab}/2) = \left(\frac{P_o}{E_i \eta}\right)\left(\frac{t_{on} + t_{off}' + t_{off}''}{t_{on} + t_{off}'}\right) - \frac{E_i t_{on} \ell}{2AN^2 \mu} \tag{44}$$

Although there are five unknowns t_{on}, t_{off}', t_{off}'', e_c, and I_b, with only four equations, one of the five unknowns is identically zero for each of the three distinct modes of operation. These three modes are discussed separately, beginning with the one corresponding to the heaviest load condition and proceeding to extremely light loads.

First Mode of Operation

In this mode of operation, the combined line and load conditions are such that flux density B_b in Fig. 3.5 is always above the residual level B_r. Therefore, $t_{off}'' = 0$. Solution of the four general equations for the remaining four unknowns yields

$$t_{on} = DE_o / E_i^2 \tag{45}$$

$$t_{off}' = DE_o / E_i(E_o - E_i) \tag{46}$$

$$e_c = E_i(E_o - E_i) \;/\; E_o \tag{47}$$

$$I_b = (P_o \;/\eta E_i) - (DE_o\ell/\; 2AE_iN^2\mu) \tag{48}$$

For a given converter operating under specified conditions, all quantities on the right-hand side of these equations are known except for the efficiency η, which must be estimated before a numerical value for I_b can be computed.

Several significant characteristics of this converter can be seen from these results. Since it is during t_{on} that the base-circuit power loss proportional to the square of e_r occurs, the rapid decrease of t_{on} with an increase of E_i as defined by equation (45) is advantageous from an efficiency viewpoint. Furthermore, from equation (48), note that I_b vanishes at

$$P_o = E_oD\ell\eta \;/2AN^2\mu \;= E_oD\eta \;/\; 2L \tag{49}$$

where $L = AN^2\mu \;/\ell$ is the inductance of the energy-storage reactor. Equation (49) defines the particular load current P_o/E_o at which the minor B-H loop of core T1 begins to include the residual point B_r. Observe that this load is independent of the input voltage E_i.

Another significant characteristic that is important from a design point of view can be seen by solving equations

(39), (40) and (45) for B_a and remembering that $t_{off}'' = 0$ in this mode. Then,

$$B_a = B_c + (\Delta B_{ab}/2) = (\mu N/\ell)(P_o/\eta E_i) + (DE_o / 2AE_iN) \quad (50)$$

Replacing E_i and P_o by their respective minimum and maximum expected values, equation (50) can be used as a constraint to choose proper parameters for the energy-storage reactor, as the resulting B_a must be restricted to a value that is less than B_s.

Figure 3.6(A) shows in the upper trace the induced voltage and in the lower trace the winding current of the energy-storage reactor that are typical of this mode of operation. Operation in this mode ceases when conditions are such that the instantaneous current in the winding becomes zero at the end of t_{off}'. Further reduction in the output load brings about operation in mode two.

Second Mode of Operation

In this mode, the combined line and load conditions are such that three distinct states of the circuit exist within each cycle. Two of these are similar to the two states that exist in the first mode of operation when the flux in T1 increases during t_{on} and decreases during t_{off}'. The new third state is initiated during the off time of Q1 when the flux

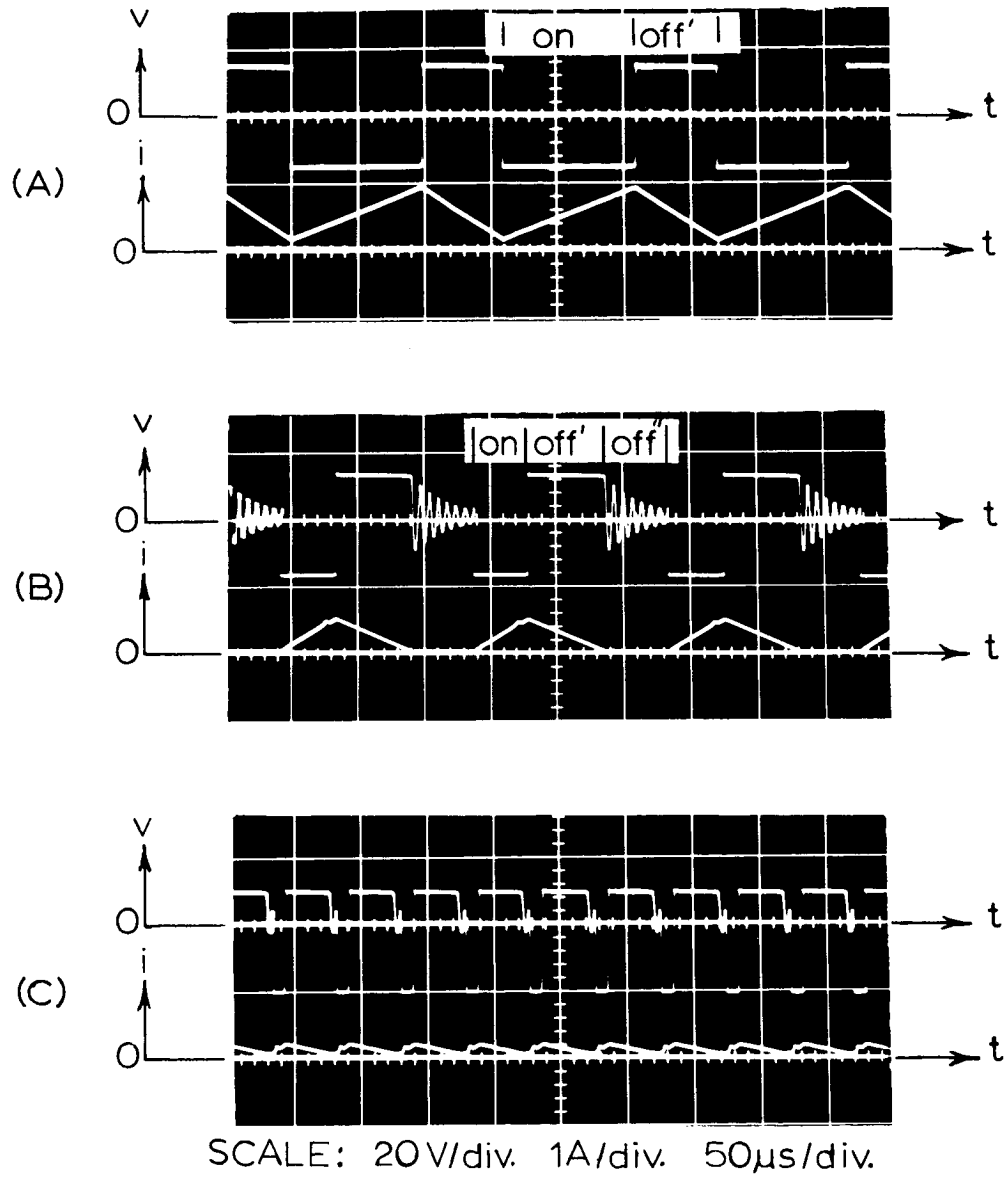

Fig. 3.6. Induced Voltage and Winding Current for the Energy-Storage Reactor.

(A) First Mode of Operation at E_i = 12 V, P_o = 6 W

(B) Second Mode of Operation at E_i = 18 V, P_o = 3 W

(C) Third Mode of Operation at E_i = 24 V, P_o = 1 W

density of T1 first reaches B_r and the current through diode D1 ceases to flow. It continues until Q1 is turned on to begin a new cycle. In this mode, the flux density B_b of Fig. 3.5 coincides with the residual level B_r. Analytically, the constraint $I_b = 0$ is applied, and the solutions of the four general equations (41), (42), (43), and (44) are:

$$t_{on} = (D / E_i) + (E_o - E_i) / E_i^2 E_o (P_o / \eta)(2L) \tag{51}$$

$$t_{off}' = D / (E_o - E_i) + (1 / E_i E_o)(P_o / \eta)(2L) \tag{52}$$

$$t_{off}'' = \frac{D}{E_i}\left(1 + \frac{DE_iE_o}{E_o - E_i} \cdot \frac{\eta}{P_o} \cdot \frac{1}{2L}\right)\left(1 - \frac{1}{DE_o} \cdot \frac{P_o}{\eta} \cdot 2L\right) \tag{53}$$

$$e_c = \frac{E_i}{1 + \left(\frac{DE_iE_o}{E_o - E_i}\right)\left(\frac{\eta}{P_o}\right)\left(\frac{1}{2L}\right)} \tag{54}$$

Notice the operating frequency $1 / (t_{on} + t_{off}' + t_{off}'')$ for this mode is not only a function of E_i, E_o, and D as it is in mode one, but also a function of the inductance L of the linear reactor and of the input power P_o / η . While both t_{on} and t_{off}' diminish with P_o, the increase of t_{off}'' due to the reduction in load is larger than the decreases of t_{on} plus t_{off}'. Therefore, the frequency decreases with a reduced load.

Figure 3.6(B) shows an oscillogram of the voltage and the current of the energy-storage reactor for this mode of operation. A point of particular significance concerning the steady-state operation of the converter is the damped high-frequency oscillation or ringing that occurs during the interval t_{off}''. A detailed description of the nature of this ringing and its effects on the normal operation of the converter are presented in Appendix C and Appendix D. While the oscillatory voltage during t_{off}'' is clearly apparent in the upper trace, the oscillatory current during this time is not discernible with the current scale used, since it is much smaller than the winding current during either t_{on} or t_{off}'.

From equation (54) it is seen that voltage e_c decreases with a reduction in load. At a certain reduced load the small e_c causes the converter to enter the next mode of operation.

Third Mode of Operation

Under conditions of very light load, voltage e_c is too small to provide the magnetizing mmf required for core T2 to reach a vertical unsaturated segment of its square-loop B-H characteristic. The flux oscillations of this core are then limited to a saturation region of the core characteristic, resulting in a transition to high-frequency mode of operation. Figure 3.6(C) shows an oscillogram of the voltage and current of the energy-storage reactor under this condition. Output regulation is still being maintained by the feedback loop. This feature of shifting into a controlled high-frequency mode at

very light loads rather than reducing the duty cycle to almost zero, which in reality means a very low conversion frequency, is important in that it enables the output-voltage ripple to remain small and minimizes the problems of selecting a proper RC lead network to provide for the stable operation of the converter at light load.

Comparison of Operating Frequencies with Other Variable-Frequency Converters

For dc to dc converters, duty-cycle control at a variable frequency generally can be achieved by causing the power switching element to have (1) variable on time and variable off time such as the converter discussed in this chapter, or (2) constant on time and variable off time, or (3) constant off time and variable on time. For each of these three types of converters, the conversion frequency is a function of the load. For heavy to medium loads corresponding to operation in mode one, the frequency is $f_A = 1 / (t_{on} + t_{off}')$; for light loads corresponding to operation in mode two, it is $f_B = 1 / (t_{on} + t_{off}' + t_{off}'')$. Based on results obtained from the analyses of these two modes of operation, the conversion frequencies for converter types (1), (2), and (3) with load conditions (A) and (B) are

$$f_{(1)A} = E_i(E_o - E_i) / DE_o^2 \qquad (55A)$$

$$f_{(1)B} = 2E_i^2 E_o G \,/\, (DE_i E_o + 2G)^2 \tag{55B}$$

$$f_{(2)A} = (E_o - E_i) \,/\, E_o t_{on} \tag{56A}$$

$$f_{(2)B} = 2G \,/\, E_i^2 E_o t_{on}^2 \tag{56B}$$

$$f_{(3)A} = E_i \,/\, E_o t_{off}' \tag{57A}$$

$$f_{(3)B} = \frac{E_i^2 E_o}{G + E_i^2 E_o M + \left[G(G - 2E_i^2 E_o M)\right]^{\frac{1}{2}}} \tag{57B}$$

where $G = (E_o - E_i)(P_o / \eta)L$, and $M = t_{off}' + t_{off}'' =$ constant off time.

In order to compare frequency ranges, equations (55A), (56A), and (57A) are plotted as curves (1), (2), and (3) in Fig. 3.7(A); and (55B), (56B), and (57B) in Fig. 3.7(B) for load condition (B). These two figures show normalized frequency f / f_{max} versus normalized input voltage E_i / E_o under the conditions of identical output voltage E_o, input power P_o / η, inductance L and input-voltage range ΔE_i for all three converters. In order to have a meaningful comparison between frequency ranges, all three converters are assumed to have the same frequency at $E_i / E_o = \frac{1}{2}$, where t_{on} and t_{off}' are equal.

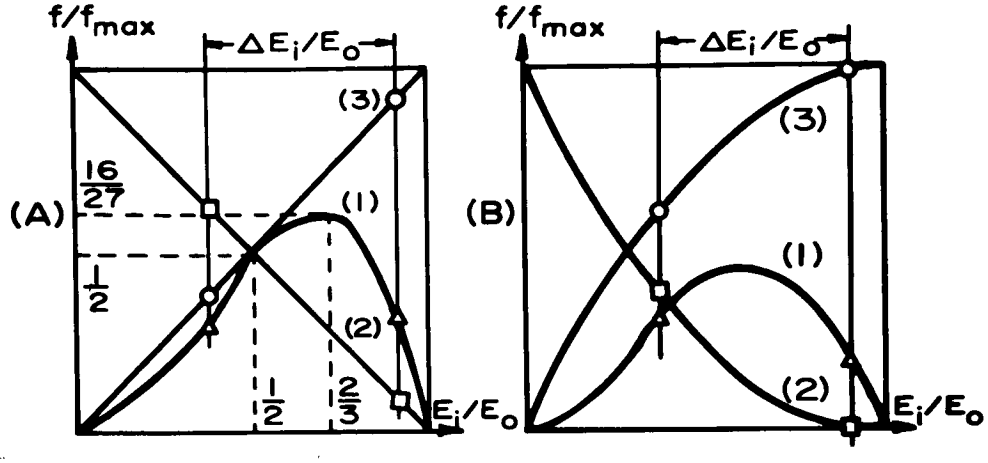

Fig. 3.7. Frequency versus Input Voltage for Different Loads.

(A) Heavy and Medium Load

(B) Light Load

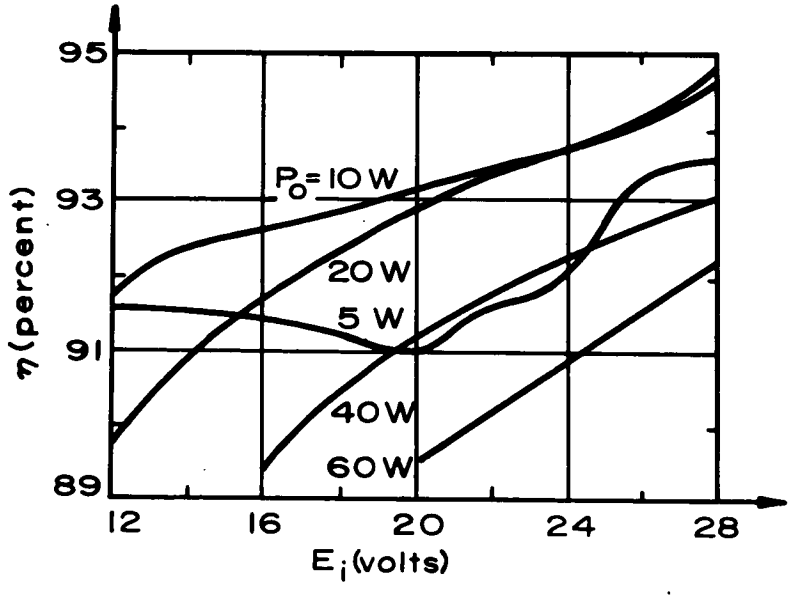

Fig. 3.8. Efficiency versus Input Voltage for Different Loads

From these figures, it can be seen that while the frequency of inverter types (2) and (3) either increase or decrease monotonically with input voltage, inverter type (1) has a maximum at a certain input voltage. Consequently, the variable-on-time variable-off-time converter has a minimum range of operating frequency for the specified line and load variation.

Performances

A 30-volt regulated dc to dc converter was designed which operates over an input-voltage range of 12 to 28 volts and an output-load variation of 0 to 20 watts. In addition, it has an output power rating of 40 watts at an input of 16 volts and 60 watts at an input of 20 volts. Efficiency as a function of input voltage and output load is plotted in Fig. 3.8. It is generally over ninety percent for the entire input-voltage range and an output-load range of 4 to 20 watts. The output-voltage regulation is within $\pm$ 0.33% of the nominal output voltage for all data points of Fig. 3.8 and down to no load over an input-voltage range of 12 to 28 volts. The peak-to-peak output ripple within the design range increases with decreasing E_i and increasing P_o. At the worst case of E_i = 12 volts and P_o = 20 watts, the ripple is 10 millivolts.

The operating frequency of the converter has a maximum point of about 9.3 kHz in mode one operation at E_i = 19 volts

and P_o = 20 watts. The absolute minimum frequency at which the converter operates occurs within mode two and is about 2.6 kHz at E_i = 14 volts and P_o = 0.45 watts. The absolute maximum frequency of the converter occurs within mode three and is found to be 50 kHz at E_i = 12 volts and P_o = 0.1 watts.

The particular load at which the first mode of operation ends is predicted by equation (49) to be 4.6 watts, assuming an efficiency of 90%. In actual performance, it varies from 4.5 watts at E_i = 12 volts to 4.9 watts at E_i = 26 volts, which is in good agreement with the theoretical value.

Future Development

By using the same voltage-to-duty-cycle encoder, the converter circuit can be modified to provide isolation between the input and the output sides of the converter. By so doing, short-circuit protection of the load is achieved without adding any series element in the output line between the converter and the load. This is due to the action of the feedback loop, which senses the short circuit and reacts in such a way as to cause voltage e_r of the asymmetrical multivibrator to be zero. With zero e_r, transistor Q1 remains blocking, which effectively turns off the converter as long as a short circuit exists across the load. Such a circuit will be developed in the near future.

In addition to the developments of new circuits, some of the other interesting topics in connection with converters using the principle of inductive-energy storage in general are:

(1) To study the migrations of the minor B-H loops of the energy-storage reactor during transient line and load conditions.

(2) Similar to the comparison of frequencies described in this chapter, to compare the weight and size of the energy-storage reactors used in regulated converters with (A) variable on time and variable off time, (B) constant on time and variable off time, (C) constant off time and variable on time.

(3) To compare analytically the weight and size between (A) a regulated converter in which the main magnetic element of its inverter stage has a linear B-H characteristic and (B) a regulated converter in which the main magnetic element in its inverter stage has a square-loop B-H characteristic. The comparison can be made under identical ranges of input voltage, output load, operating frequency, and identical output-ripple specifications. In essence, the comparison is made between the weight and size of the energy-storage reactor in (A) and the combined weight and size of the square-loop core plus the filter inductor in (B).

Conclusion

A dc to dc regulated converter employing duty-cycle control with variable on time and variable off time has been described. Since the on-time interval, which is the interval during which the loss in the base circuit of the power transistor occurs, decreases with either an increase in input voltage or a decrease in output load, high efficiencies over ninety percent were obtained for the test circuit with input-voltage range of 12 to 28 volts and an output-load range of 4 to 20 watts. The physical simplicity of this converter, made possible in large measure by the unconventional voltage-to-duty-cycle encoder, is attractive from a reliability and cost viewpoint. Despite its lack of physical complexity and its small size and low weight, the converter nevertheless provides small output ripple, good regulation, and considerable design flexibility, features normally found only in more complicated and bulky circuits. With both the on time and the off time of the main switching transistor being controlled by the asymmetrical multivibrator, the frequency range over which this converter operates is smaller than those of other variable-frequency converters with either constant on time or constant off time. The smaller frequency range makes it less difficult to make the proper compromises among the various performance characteristics involving size, weight, efficiency, stability, and ripple, thereby contributing materially to the good overall performance of the converter. Due to the wide range of control

provided by the asymmetrical multivibrator, the converter should be particularly suited for operating under conditions of widely changing input voltage and output load.

CHAPTER IV

A SELF-REGULATED DC TO SINE-WAVE STATIC INVERTER USING TECHNIQUES OF HIGH-FREQUENCY PULSE-WIDTH MODULATION

In certain space applications such as that of supplying power to synchronous motors and servo motors, a requirement often placed on the dc to ac inverter is that the output voltage of the inverter be a sine wave. A major concern in designing static dc to sine-wave inverters has been the weight and size of the output transformers and the output filter components. Often they have been dictated by the low frequency of the sinusoidal output voltage which typically is 400 hertz.[23] Significant reduction in the size and weight of output filters can be effected through the use of digital techniques and by employing special output-transformer connections to synthesize a stepped wave which closely approximates a sine wave and thus requires a minimum of filtering.[5,6] However, these approaches usually involve rather complex circuits, and inherently require a heavy and bulky output transformer because it must process the output power of the inverter at the desired low frequency.

More recent developments in dc to sine-wave inverters have eliminated the requirements for both the output transformers and the low-frequency filter components by utilizing the technique of pulse-width modulation. Here, the desired low-frequency

sinusoidal output voltage is extracted from a repeating pattern of alternating high-frequency square pulses all having equal amplitudes. The widths of successive pulses in the pattern are controlled to vary sinusoidally in accordance with a reference sinusoidal signal of the desired output frequency. Although it may be intuitively asserted and experimentally supported that in such square-wave patterns the amplitudes of the first few harmonics of the fundamental frequency can be made very small, no rigorous mathematical proof of the fact seems to have been documented.

Described in this chapter are a circuit and some analytical findings about a physically simple dc to sine-wave inverter using the technique of pulse-width modulation. The aforementioned assertion concerning the small amplitudes of harmonics is analytically proved, thus providing a mathematical foundation for the technique of pulse-width modulation. The physical simplicity of this inverter is attractive from a reliability viewpoint. It requires no power transformer and no low-frequency filter components to accomplish the desired dc to sinusoidal ac transformation, thereby reducing substantially the size and weight of the inverter. The versatility of this inverter configuration is further enhanced by its self-regulating property, which keeps an essentially constant sinusoidal output voltage under large dc input-voltage variations.

In the following sections, a brief historical review of the developments of static dc to sine-wave inverter is given first, followed by the circuit description of the self-regulating

inverter. Mathematical analyses are then performed to prove the self-regulating property of this particular inverter and the small amplitudes of the harmonics. Finally, a test circuit and its performance characteristics are shown to substantiate the theories developed in this chapter.

Historical Review of the Developments of Static Dc to Sine-Wave Inverters

The possible operating modes of the transistors or other solid-state devices used in static dc to sine-wave inverters generally may be classified as either dissipative or nondissipative. For minimum harmonic distortion in the dissipative mode of operation, the operating points of the transistors are in the linear regions of i-v characteristics.[24] Large power dissipation in the semiconductors results in very low efficiency, which is not practical for static inverters aboard spacecrafts except when only a small amount of power is involved. In the nondissipative type of operation, the semiconductor devices usually are switched fully on or fully off. Thus, the average power dissipated by the switches is usually very small compared to the total power switched.

The simplest nondissipative type of inverter would be one of the self-oscillating magnetically-coupled multivibrators such as the circuits by Royer[4] or Van Allen[25] which gives a square-wave output voltage. The harmonic components present in the output of these inverters are the fundamental and all odd harmonics. Fourier analysis of a square wave shows that

there exist 33% third harmonic and 20% fifth harmonic.[26] Since these harmonics are so close to the fundamental frequency, a rather heavy and bulky ac filter is required to extract the fundamental sinusoidal component. The size and weight problem is further aggravated by the output transformer, which must handle the entire output power of the inverter at the desired low fundamental frequency.

In higher power inverters, a number of switches with conduction intervals starting at different phase positions may be employed to reduce harmonics. This is practical because multiple switches are required ultimately to deliver the large rated power output. Digital techniques and unique transformer connections[5,6] have been utilized to shape the output voltage into a stepped wave such as that shown in Fig. 4.1. The stepped waveform is obtained by adding the outputs of a number of flip-flop circuits that switch in a predetermined sequence at equal time intervals. The height of each step is set to be equal to the corresponding average of the simulated sine waves in that step interval. The harmonic content is reduced and is a function of the number of steps. Fourier expansion of this type of waveform shows that when the stepped wave is properly formed, the first harmonic present is one less than the number of steps per cycle.[6] Although this stepped wave requires little filtering due to its small harmonic content, the generation of this stepped wave inherently requires a power transformer whose size and weight are still dictated by the desired output

frequency of the load. Furthermore, the large number of power-handling semiconductor switches and their associated control circuits tend to reduce the reliability of the inverter.

One circuit configuration which eliminates the need for low-frequency power transformer employs the square-wave output of a low-power magnetically-coupled multivibrator such as the Royer circuit or the Van Allen circuit to drive four power transistors or SCRs of a bridge chopper at the desired output frequency. The basic schematic diagram of a bridge chopper is shown in Fig. 4.2.[27] Input power to the bridge is supplied by a dc source V at the proper voltage level, which could be the output of a dc to dc converter operated at very high frequencies. The square-wave outputs of the low-power multivibrators are then applied to the base circuits of the four transistors in the bridge chopper in such a way as to cause each of the two diagonal transistor pairs to conduct simultaneously for a half cycle. Consequently, a square-wave voltage appears across the load resistance R_L. The amplitude of voltage V and the amount of power that can be supplied to the load are limited only by the electrical characteristics of the transistors. While the low-frequency power transformer is not needed here, the requirement of the ac filters is unchanged from the square wave as the load voltage is still a symmetric square wave.

Another scheme which utilizes the basic bridge-chopper circuit of Fig. 4.2 has been reported that effectively eliminates the third and the fifth harmonics present in the ac load-voltage waveform of a bridge chopper.[28] This is accomplished

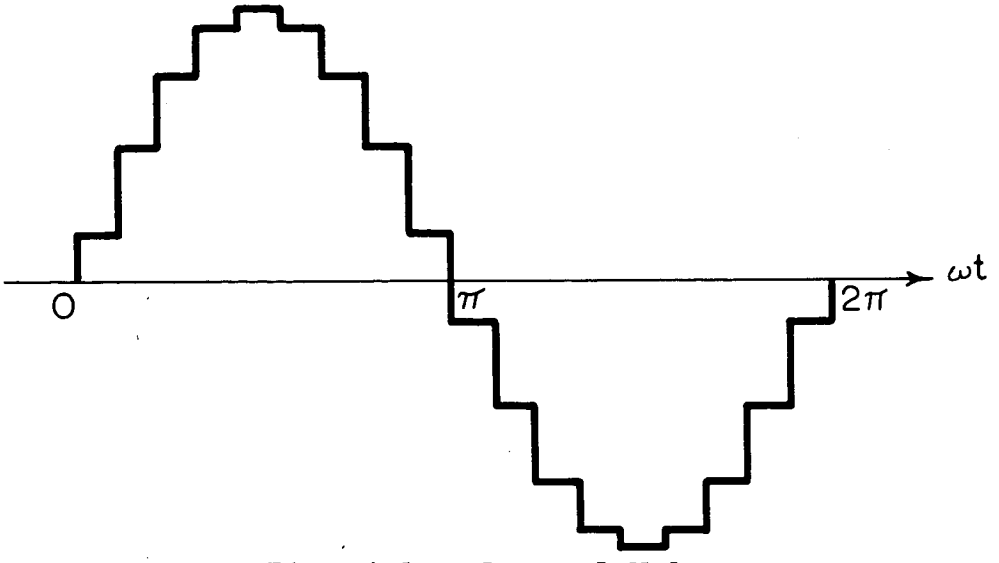

Fig. 4.1. Stepped Voltage.

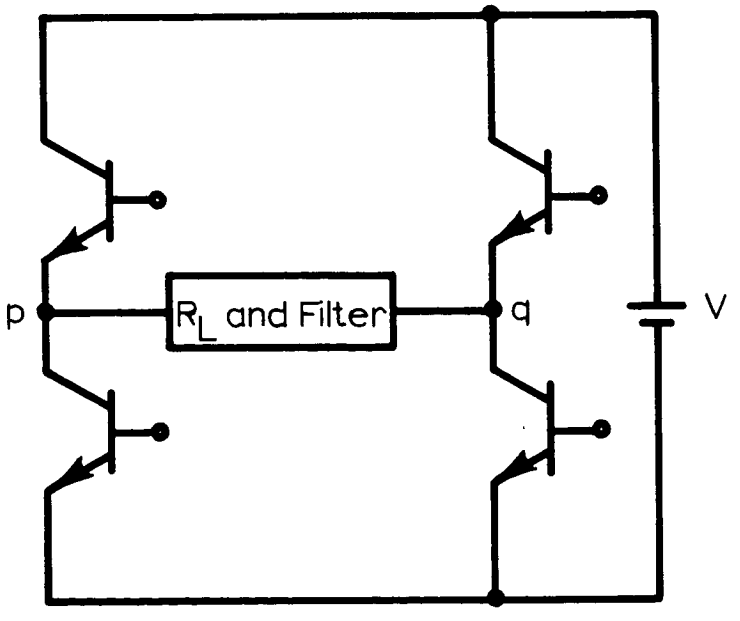

Fig. 4.2. Bridge Chopper.

by generating five cycles of controlled asymmetric square waves within one load-voltage cycle of the desired fundamental frequency, such as that shown in Fig. 4.3. However, when compared with a single symmetric square wave of the same amplitude, elimination of the third and fifth harmonics of this inverter is frequently accompanied by an increase of almost two times in the seventh harmonic and five times in the ninth harmonic. While the seventh and the ninth harmonics are easier to attenuate as compared to the third and the fifth, the filter components required are still heavier and more bulky than those of the recently-developed inverters using the pulse-width modulation technique.[7,29]

While the digital stepped-wave inverters mentioned earlier generate voltage steps of different amplitudes at equal time intervals, the inverters with pulse-width modulation generate voltage pulses of different time intervals all at equal amplitudes such as that shown in Fig. 4.4. In practice, the stepped-wave inverters use many semiconductors that switch only once each load-voltage cycle, while the inverters with pulse-width modulation employ a few semiconductors that switch many times during each power-frequency cycle. In this type of modulation, a small-power sinusoidal signal with a frequency identical to the desired frequency of the sinusoidal output voltage of the inverter is used in a certain control circuit to generate pulses. The widths of these pulses are proportional to the sinusoidal modulating-signal level. The frequencies of the pulses are much higher than the desired frequency of the sinusoidal output voltage of the inverter. These variable-

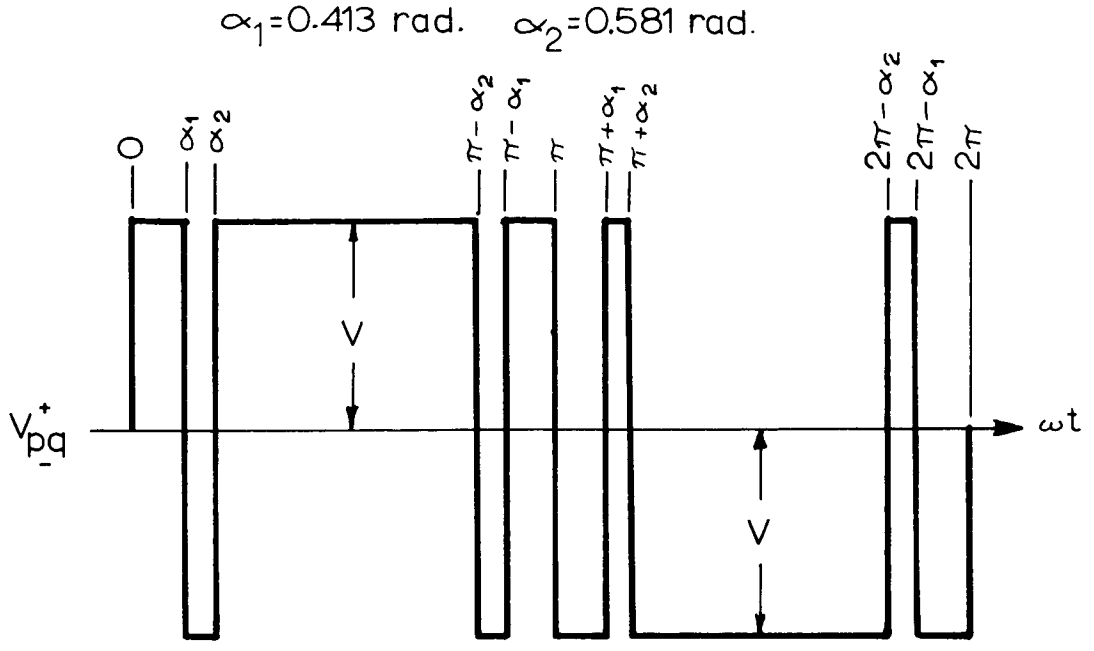

Fig. 4.3. Voltage Waveform Without Third and Fifth Harmonics.

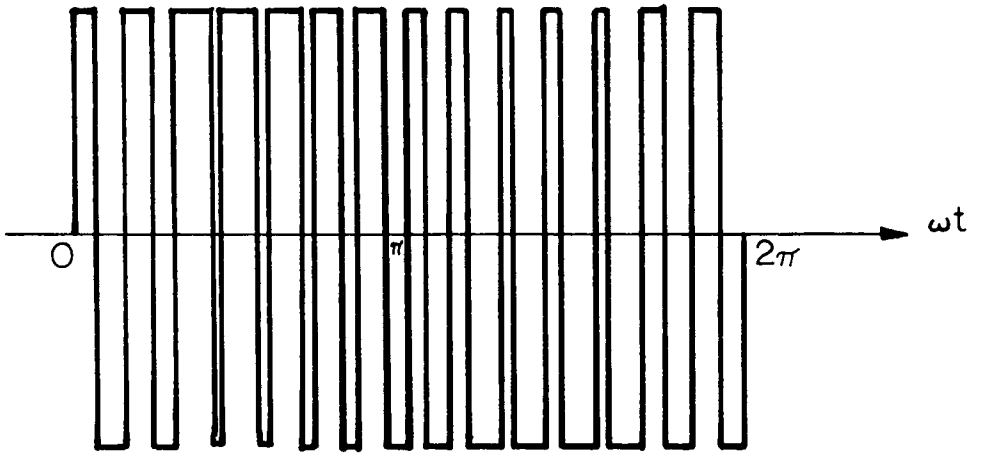

Fig. 4.4. Pulse-Width Modulated Square Pulses.

width pulses are then used to control the basic bridge-chopper circuit of Fig. 4.2. Since the amplitudes of all odd harmonics of the low-frequency sinusoidal output voltage that are below the frequencies of the pulses are small, the filtering requirement of the high-power output voltage of the bridge chopper is limited to the attenuation of harmonics at the high frequencies of the pulses. This results in size and weight savings in the output filter. Also, since the direct-voltage source which supplies the major portion of the input power to the inverter is connected directly across the bridge chopper, and that the amplitude of this voltage is predetermined and obtained from a high-frequency dc to dc converter to provide the sinusoidal output voltage of the inverter with the desired amplitude, no low-frequency power transformer is inherently needed in this configuration. Regulation of the sinusoidal output voltage across the load of the bridge chopper can be achieved by controlling the input voltage to the bridge chopper (the output of the dc to dc converter) in a closed-loop fashion.

This chapter describes a physically simple, open-loop regulated dc to sine-wave inverter using the technique of pulse-width modulation. In the control circuit of this inverter, high-frequency pulses whose widths are modulated by a sine-wave signal are obtained through a simple switching control consisting of two transistors and a square-loop core. The properly modulated signals of small voltage and small power are then used to control the power transistors in the large-power bridge chopper. Descriptions of the circuit and its functions are given in the following sections.

Circuit Description

The inverter is composed of two sections as shown in Fig. 4.5. A low-power pulse-width modulator with four output windings N5 to N8 supplies base drives to four power transistors in the bridge chopper containing the load R_L and the LC filter.

High-Frequency Pulse-Width Modulator

This is a magnetically-coupled multivibrator with a saturable core T1 and transistors Q1 and Q2. Direct voltage 2E is divided into two equal parts across C1 and C2 for the two halves of the multivibrator. An externally-generated reference sinusoidal voltage with amplitude $M < E$ and period $2\pi/\omega$ is inserted in series with each half of the multivibrator. When Q1 conducts, voltage e_1 across N1 is $M \sin \omega t + E$. When Q2 conducts, voltage e_2 across N2 = N1 = N is $M \sin \omega t - E$. Core T1 is chosen to have a saturation flux ϕ_s such that the maximum time required for a complete reversal of flux in core T1 is $2N\phi_s/(E-M) \ll 2\pi/\omega$. Many high-frequency pulses are thus generated in each of the output windings N5 to N8 within a fundamental period $2\pi/\omega$ of the reference sinusoidal signal. The amplitudes of similar voltage pulses across N1 or N2 form sinusoidal envelopes $M \sin \omega t \pm E$, and the widths of successive pulses vary inversely with the amplitudes of the envelopes. A representative series of such pulses within a low-frequency cycle is shown in Fig. 4.6(A). Because of the small amount of power involved in the pulse-width modulator, its weight and size

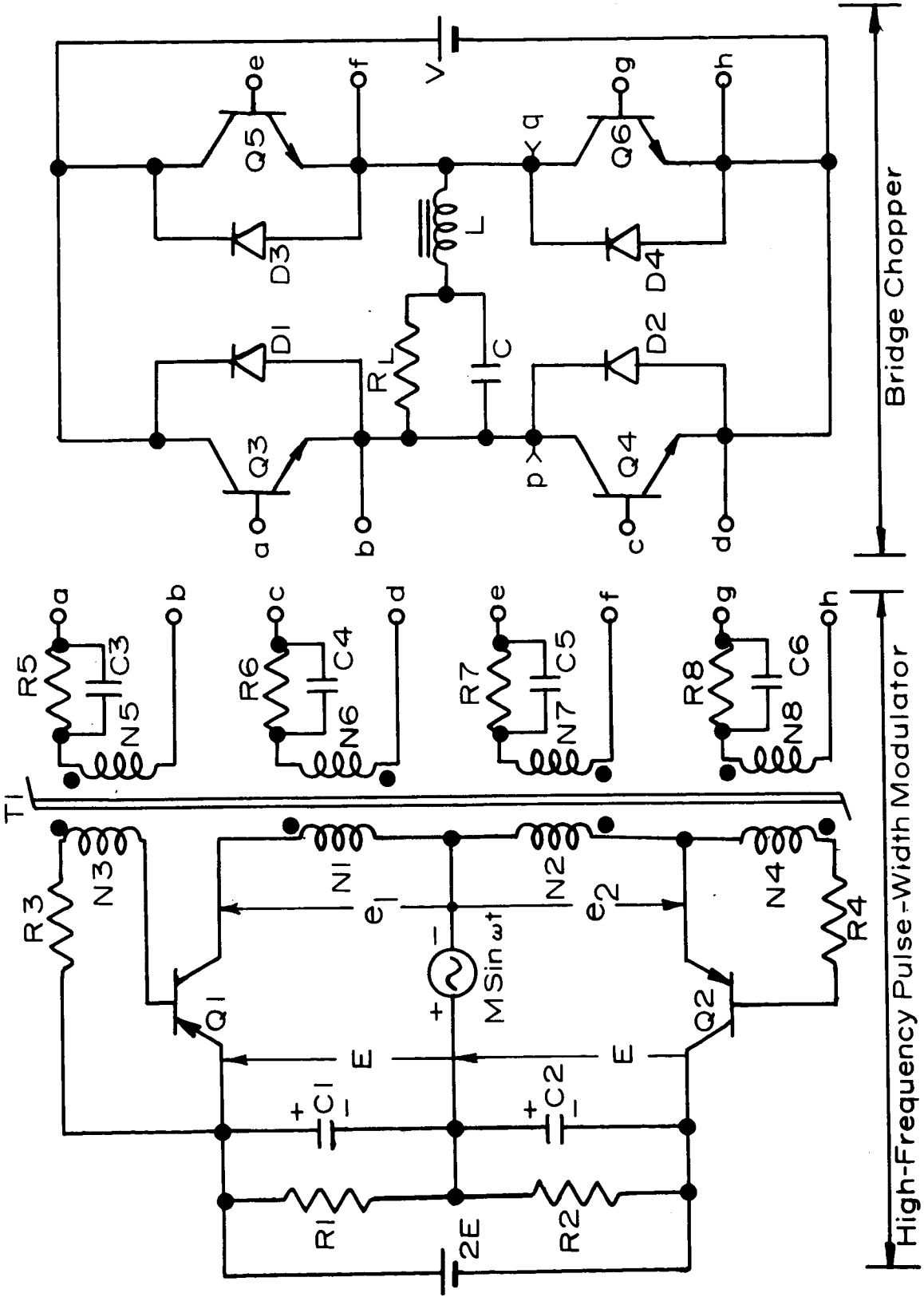

Fig. 4.5. Complete Dc to Sine-Wave Inverter.

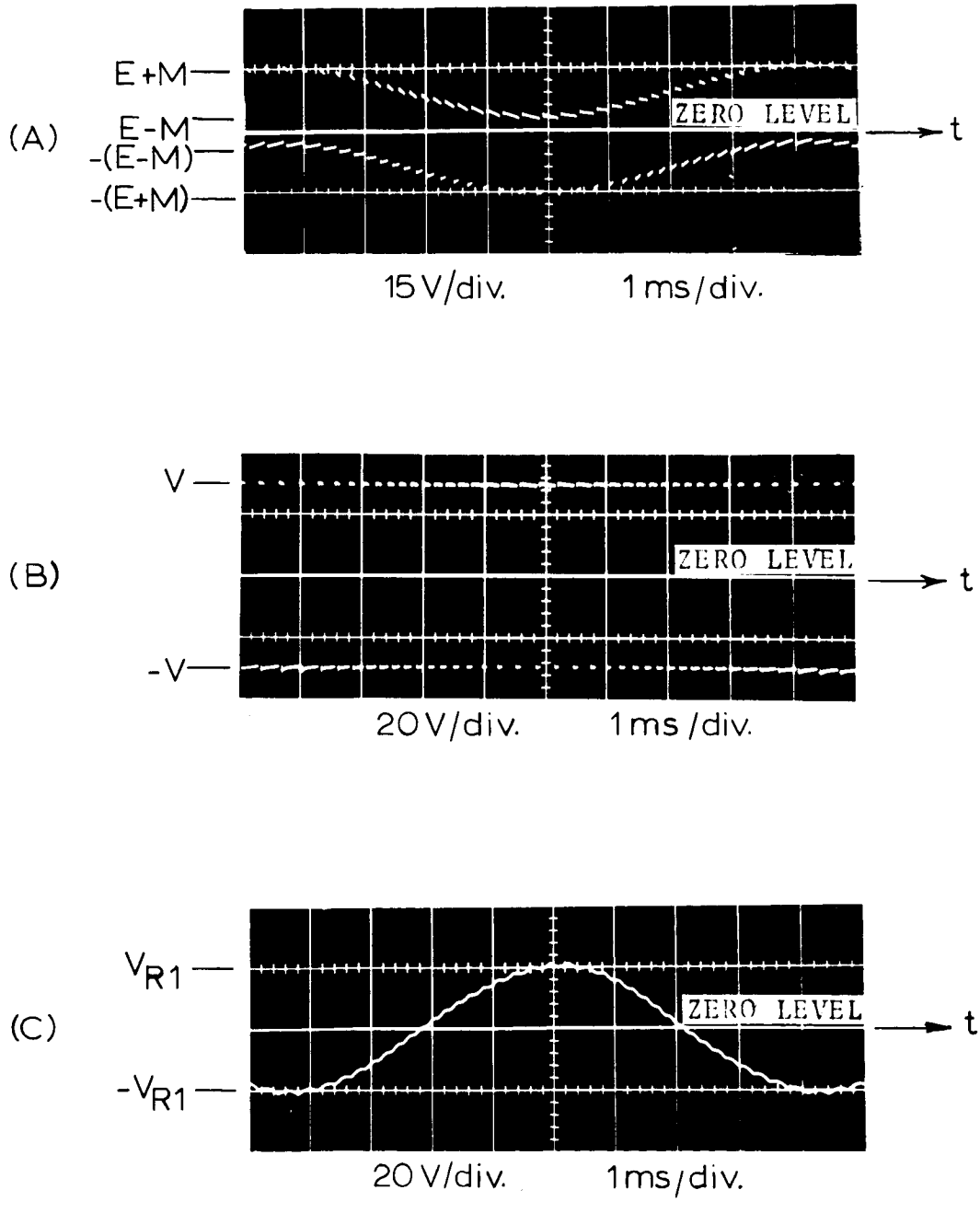

Fig. 4.6. Base-Drive Voltage, Filtered and Unfiltered Load Voltage.

(A) Voltage el
(B) Unfiltered Load Voltage V_{pq}
(C) Filtered Load Voltage

as well as its power loss are very small.

Bridge Chopper

It is clear from the winding polarities in Fig. 4.5 that the conduction of transistors Q3 and Q6 in the bridge is synchronous with that of Q1 in the modulator. Similarly, Q4 and Q5 conduct simultaneously with Q2. With input voltage V across two of the bridge terminals, the voltage v_{pq} across the other two terminals p and q is the pattern of high-frequency pulses with amplitude -V to V as shown in Fig. 4.6(B). The fundamental frequency of v_{pq} is $\omega/2\pi$. So long as the number of cycles of high-frequency pulses within $2\pi/\omega$ is very large, it is proven analytically that the amplitudes of all odd harmonics below the switching frequencies are negligible. Thus, a very small low-pass LC filter between p and q is sufficient to extract the desired sinusoidal output voltage of amplitude V_{R1} across the load R_L (see Fig. 4.6(C)). The four diodes D1 to D4 provide paths for the reactive currents due to the presence of the filter inductor and, if any, the load inductance, thereby eliminating the possibility of high-voltage transients and waveform distortions.

Theory of Operation

In the following mathematical analysis, the number of cycles of high-frequency pulses within $2\pi/\omega$ is first analyzed. Voltage V_{R1} is then calculated in terms of the input voltages

E, M, and V. The harmonics of the fundamental load voltage that are below switching frequencies are then proved to be negligible. Finally, recurrence formulas employed in the computer analysis of harmonics are presented. Throughout the mathematical derivations, the assumption of ideal components with negligible voltage drop across them is made. Also, the frequencies of the modulated pulses are assumed to be much higher than that of the externally-generated sinusoidal signal so that the period of a pulse cycle is significantly smaller than $2\pi/\omega$.

Figure 4.7 shows the amplitudes of the instantaneous voltages e_1 and $-e_2$ across the two primary windings N1 and N2 of the pulse-width modulator. To trace a cycle of high-frequency pulse within the low-frequency cycle, assume that transistor Q2 starts to conduct at $t = \theta_{2n-2}/\omega$ when the flux of the square-loop core is at positive saturation. Voltage $-e_2$ with amplitude $|-e_2|$ across N2 starts the downward flux excursion of the core, which has a fixed volt-second capacity D. Let the time be θ_{2n-1}/ω when the core reaches negative saturation. The area under $|-e_2|$ between θ_{2n-2}/ω and θ_{2n-1}/ω is therefore equal to D. Analytically,

$$\int_{\theta_{2n-2}/\omega}^{\theta_{2n-1}/\omega} (E - M \sin \omega t)\,dt = D \qquad (58)$$

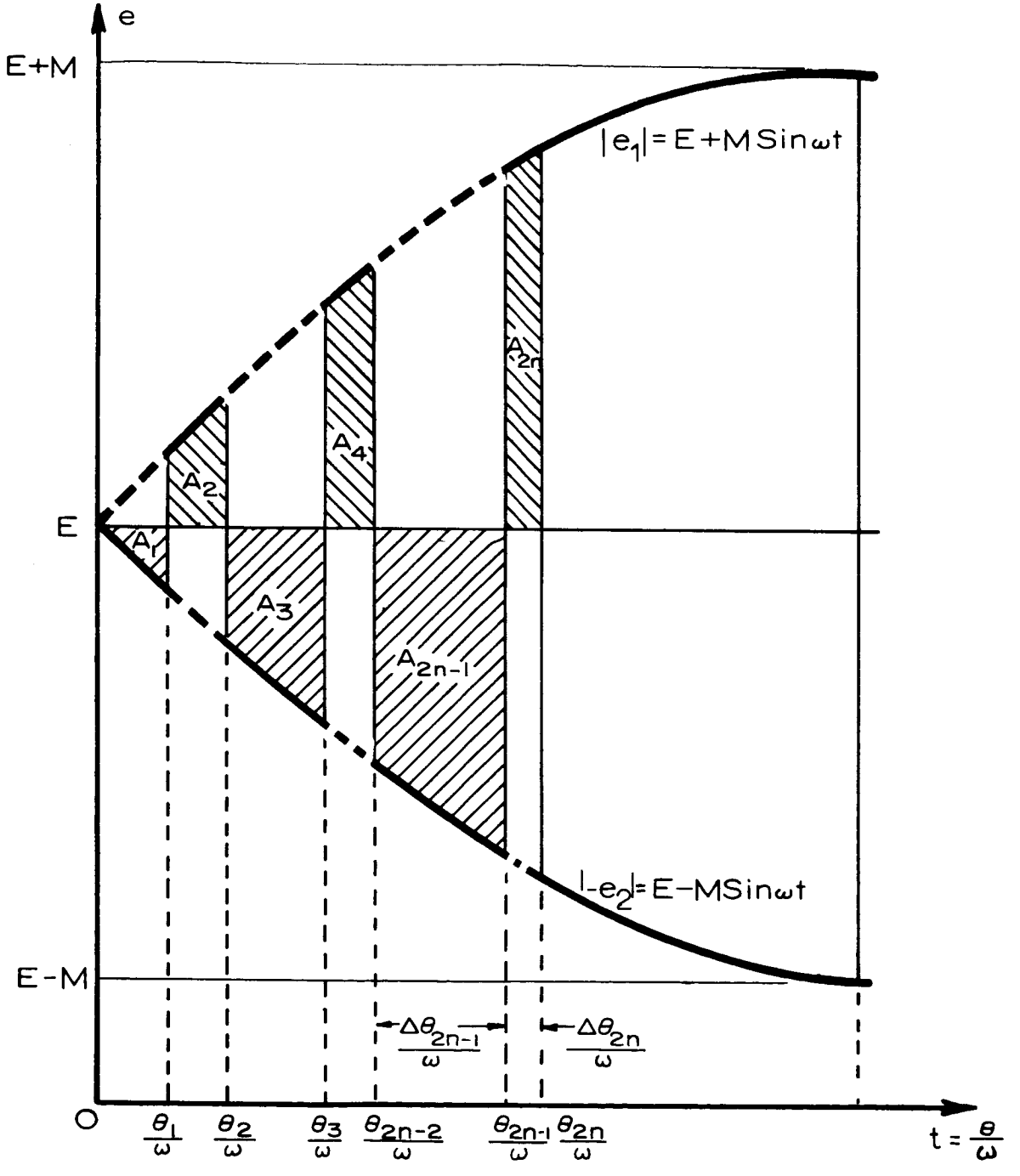

Fig. 4.7. Pulse-Width Modulation.

The saturation of the core at $t = \theta_{2n-1}/\omega$ initiates the turn off of Q2 and the turn on of Q1. Voltage $E + M \sin \omega t$ is now impressed across N1, and upward flux excursion begins and continues until positive saturation is reached at $t = \theta_{2n}/\omega$,

$$\int_{\theta_{2n-1}/\omega}^{\theta_{2n}/\omega} (E + M \sin \omega t)\,dt = D \qquad (59)$$

Start at $t = \theta_{2n-2}/\omega$ when the core is at positive saturation; its flux decreases and reaches the negative saturation at θ_{2n-1}/ω, and then increases and returns to the positive saturation at $t = \theta_{2n}/\omega$. During these processes the time consumed is $(\frac{\theta_{2n}}{\omega} - \frac{\theta_{2n-2}}{\omega}) << \frac{2\pi}{\omega}$. This describes how one cycle of high-frequency pulse is generated within $2\pi/\omega$.

Number of High-Frequency Cycles Within One Low-Frequency Cycle

From Fig. 4.7 the total volt-seconds consumed by the square-loop core over a complete low-frequency cycle is

$$(2\pi E/\omega) - (A_1 - A_2 + A_3 - A_4 + \ldots.) \qquad (60)$$

where the A's are the shaded areas in Fig. 4.7 in which

$$A_{2n-1} = (M/\omega)(\cos\theta_{2n-2} - \cos\theta_{2n-1}) \tag{61A}$$

$$A_{2n} = (M/\omega)(\cos\theta_{2n-1} - \cos\theta_{2n}) \tag{61B}$$

where n = 1, 2, 3,...., and $\theta_o = 0$. From Fig. 4.7, if the widths of the areas are small compared to $2\pi/\omega$ so that the areas A_{2n-1} and A_{2n} can be considered to have the same height M sin θ_{2n-1}, then, the odd area A_{2n-1} is generally larger than the successive even area A_{2n} because of the longer time associated with A_{2n-1} for the core to saturate. Consequently, the term $(A_1 - A_2 + A_3 - A_4 + ...)$ in equation (60) is always positive. The total volt-seconds consumed by the core within $2\pi/\omega$ is therefore maximum at M = 0 where $A_1 = A_2 = A_3 = A_4 = ... = 0$, and diminishes with an increasing amplitude of M. Let the net area loss due to the modulation of M sin ωt over a complete low-frequency cycle be A_L. Then, since A_L is four times the area loss over a quarter cycle from $\theta = 0$ to $\theta = \pi/2$,

$$A_L = \sum(A_{2n-1} - A_{2n}) = (4M/\omega)(1 - 2\cos\theta_1 + 2\cos\theta_2 - .... + \cos\frac{\pi}{2}) \tag{62}$$

We now proceed to evaluate the sum of the cosine series in equation (62). First, eliminating D from equations (58) and (59) and integrating,

$$E(\theta_{2n-1} - \theta_{2n-2}) - E(\theta_{2n} - \theta_{2n-1}) = M(\cos\theta_{2n-2} - \cos\theta_{2n}) \tag{63}$$

Replacing θ_{2n-2} by $(\theta_{2n-1} - \Delta\theta_{2n-1})$ and θ_{2n} by $(\theta_{2n-1} + \Delta\theta_{2n})$, equation (63) becomes:

$$E(\Delta\theta_{2n-1} - \Delta\theta_{2n}) = M(\cos\theta_{2n-1}\cos\Delta\theta_{2n-1} + \sin\theta_{2n-1}\sin\Delta\theta_{2n-1}) - M(\cos\theta_{2n-1}\cos\Delta\theta_{2n} - \sin\theta_{2n-1}\sin\Delta\theta_{2n}) \quad (64)$$

Due to the large number of high-frequency pulses within a low-frequency cycle, the angles $\Delta\theta_{2n-1}$ and $\Delta\theta_{2n}$ are extremely small. Approximating the sine and cosine of these angles by the angles themselves and unity respectively, equation (64) becomes

$$E(\Delta\theta_{2n-1} - \Delta\theta_{2n}) \approx M\sin\theta_{2n-1}(\Delta\theta_{2n-1} + \Delta\theta_{2n}) \quad (65)$$

Also from Fig. 4.7, under the conditions of small $\Delta\theta_{2n-1}$ and $\Delta\theta_{2n}$, the areas A_{2n-1} and A_{2n} can be treated as rectangles of equal height $M\sin\theta_{2n-1}$ with the dc voltage level E as the common base. Then,

$$A_{2n-1} - A_{2n} \approx \left[(M\sin\theta_{2n-1})/\omega\right](\Delta\theta_{2n-1} - \Delta\theta_{2n}) \quad (66)$$

From equations (65) and (66),

$$A_{2n-1} - A_{2n} \approx (M^2/E\omega)(\sin^2\theta_{2n-1})(\Delta\theta_{2n-1} + \Delta\theta_{2n}) \qquad (67)$$

Consequently, over a complete low-frequency cycle, the net area loss A_L becomes

$$A_L = \sum (A_{2n-1} - A_{2n}) \approx \int_0^{\pi/2} 4(M^2/E\omega)\sin^2\theta \, d\theta = \pi M^2/E\omega \qquad (68)$$

The approximate volt-seconds consumed by the core over a low-frequency cycle $2\pi/\omega$ is therefore $(2\pi E/\omega) - (\pi M^2/E\omega)$, where $(2\pi E/\omega)$ is the area that would have been consumed over the same time interval had the amplitude M of the modulating signal been zero. Let $n_o = \pi E/2\omega N\phi_s$ be the number of high-frequency cycles corresponding to $M = 0$ and n_a be that with $M \neq 0$. Then,

$$n_a = n_o \left(\frac{\frac{2\pi E}{\omega} - \frac{\pi M^2}{\omega E}}{\frac{2\pi E}{\omega}}\right) = (\pi E/2\omega N\phi_s)\left[1 - \tfrac{1}{2}(M/E)^2\right] \qquad (69)$$

Therefore, the number of high-frequency pulses within $2\pi/\omega$ decreases with either an increase in the amplitude M of the sinusoidal signal or a decrease in dc voltage E.

Fundamental Component of Load Voltage

Since the four transistors of the bridge chopper are driven by the outputs of the pulse-width modulator, and since the chopper has a dc input voltage V, the voltage between points p and g of the bridge chopper has the waveform of Fig. 4.8. Transistors Q4 and Q5 conduct simultaneously between the time intervals θ_{2n-2}/ω and θ_{2n-1}/ω, while transistors Q3 and Q6 conduct from θ_{2n-1}/ω to θ_{2n}/ω.

Fourier analysis of Fig. 4.8 shows that the zero-to-peak amplitude V_{R1} of the fundamental component is

$$V_{R1} = (4V/\pi)\left|(1 - 2\cos\theta_1 + 2\cos\theta_2 - \ldots + \cos\frac{\pi}{2})\right| \quad (70)$$

However, from equations (62) and (68),

$$\left|(1 - 2\cos\theta_1 + 2\cos\theta_2 - \ldots + \cos\frac{\pi}{2})\right| \approx \pi M/4E \quad (71)$$

Combining equations (70) and (71), the peak fundamental load voltage is

$$V_{R1} \approx (V/E)M \quad (72)$$

The frequency of the load voltage is identical to that of the modulating sine wave M sin ωt of the pulse-width modulator.

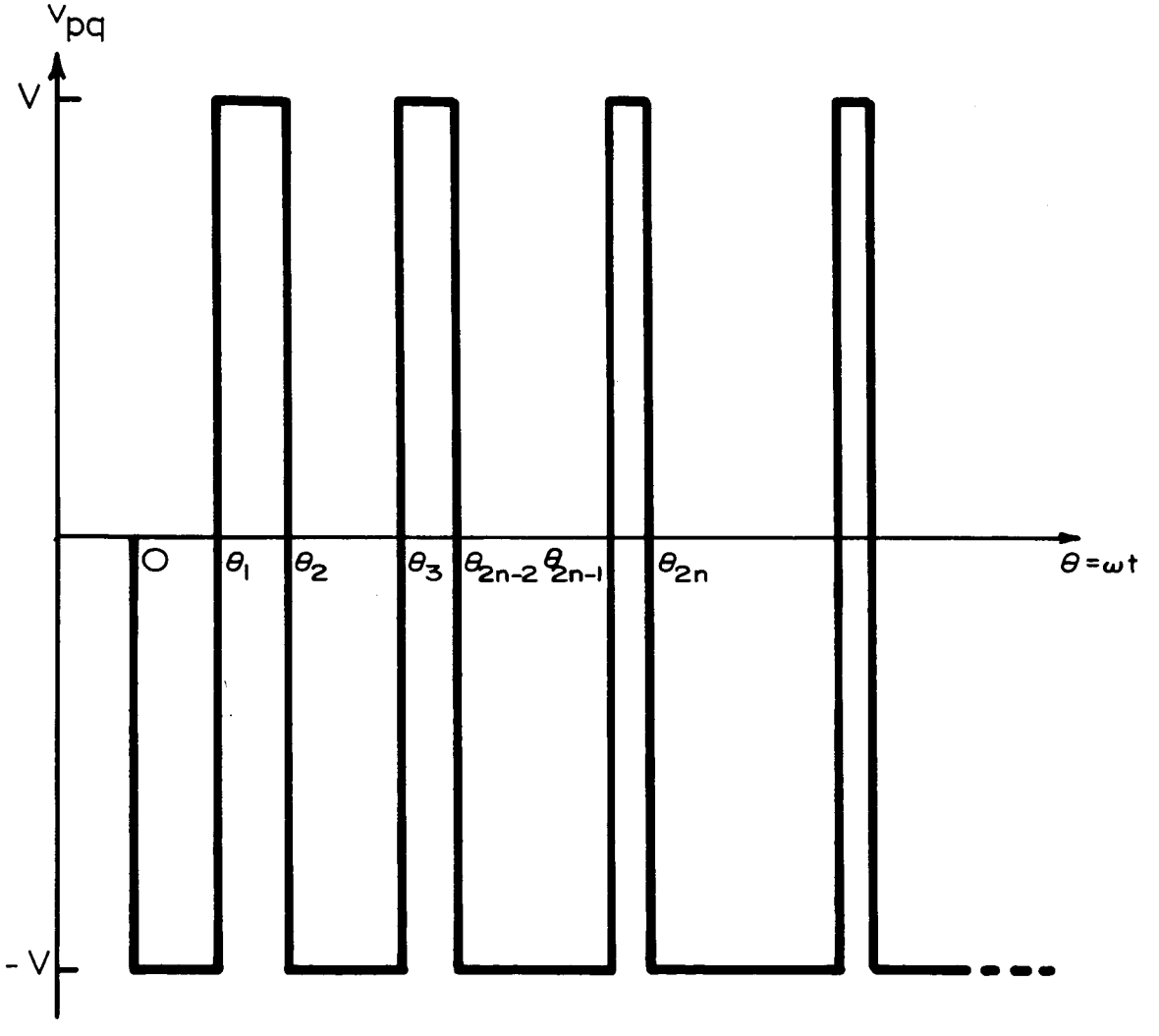

Fig. 4.8. Unfiltered Load Voltage of the Inverter.

Harmonic Analysis

Fourier analysis of Fig. 4.8 shows that the peak amplitude of the k^{th} odd harmonic is

$$V_{Rk} = (4V/\pi k)\left|(1 - 2\cos k\theta_1 + 2\cos k\theta_2 - \ldots + \cos\frac{k\pi}{2})\right| \quad (73)$$

where k = 3, 5, 7, ... etc. The algebraic sum of the cosine series in equation (73) can be calculated with the help of Fig. 4.9. In Fig. 4.9, A_{2n-1} and A_{2n} are areas below the fundamental sine wave P sin θ, where P is an arbitrary peak voltage for the fundamental. Area A_{2n-1}' and A_{2n}' are those between the fundamental sine wave P sin θ and the fictitious k^{th} harmonic P sin kθ. Analytically,

$$(A_{2n-1} - A_{2n}) + (A_{2n-1}' - A_{2n}') = (A_{2n-1} + A_{2n-1}') - (A_{2n} + A_{2n}')$$

$$= \int_{\theta_{2n-2}/\omega}^{\theta_{2n-1}/\omega} P \sin k\theta \, d\theta - \int_{\theta_{2n-1}/\omega}^{\theta_{2n}/\omega} P \sin k\theta \, d\theta$$

$$= (P/k\omega)\cdot(\cos k\theta_{2n-2} - 2\cos k\theta_{2n-1} + \cos k\theta_{2n}) \quad (74)$$

Therefore, over a quarter cycle,

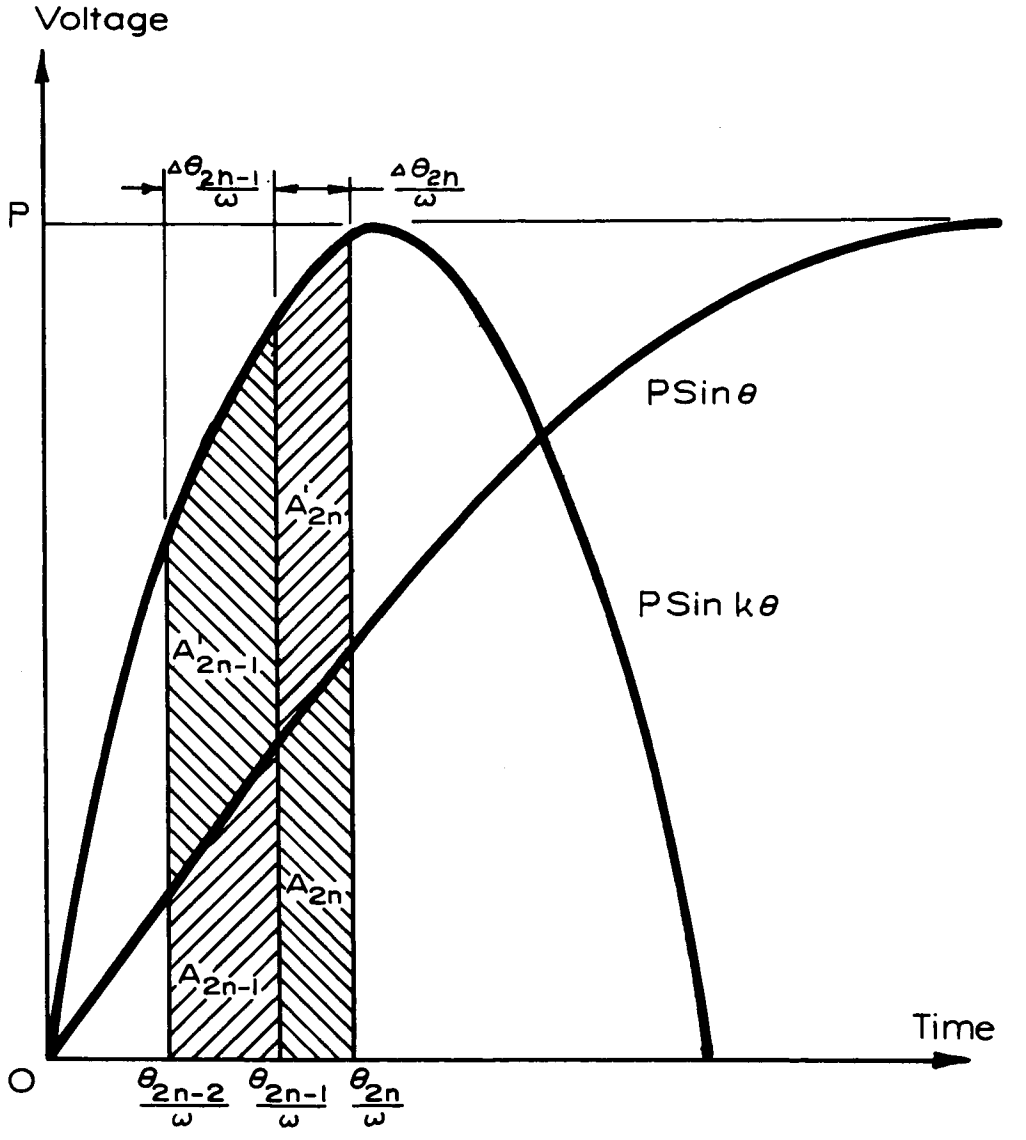

Fig. 4.9. Harmonic Analysis.

$$\Sigma(A_{2n-1} - A_{2n}) + \Sigma (A_{2n-1}' - A_{2n}')$$

$$= (P/k\omega)\cdot(1 - 2\cos k\theta_1 + 2\cos k\theta_2 - .... + \cos\frac{k\pi}{2}) \quad (75)$$

The combination of equations (73) and (75) yields

$$V_{Rk} = (4V\omega/\pi P)\left| \Sigma (A_{2n-1} - A_{2n}) + \Sigma(A_{2n-1}' - A_{2n}')\right| \quad (76)$$

The problem of determining V_{Rk} thus becomes that of solving for $\Sigma (A_{2n-1} - A_{2n}) + \Sigma(A_{2n-1}' - A_{2n}')$. In the following derivations, the two summation terms in equation (76) are solved separately, using again Fig. 4.9.

If $\Delta\theta_{2n-1}$ and $\Delta\theta_{2n}$ are negligibly small in Fig. 4.9, the areas A_{2n-1}' and A_{2n}' may be considered as rectangles with common height $P(\sin k\theta_{2n-1} - \sin\theta_{2n-1})$. Therefore,

$$A_{2n-1}' - A_{2n}' \approx (P/\omega)(\sin k\theta_{2n-1} - \sin\theta_{2n-1})(\Delta\theta_{2n-1} - \Delta\theta_{2n}) \quad (77)$$

Combining equations (65) and (77),

$$A_{2n-1}' - A_{2n}' \approx$$

$$(MP/E\omega)(\sin k\theta_{2n-1} \sin\theta_{2n-1} - \sin^2\theta_{2n-1})\cdot(\Delta\theta_{2n-1} + \Delta\theta_{2n}) \quad (78)$$

Consequently, over a quarter cycle,

$$\Sigma(A_{2n-1}' - A_{2n}') \approx (MP/E\omega)\int_0^{\pi/2} (\sin k\theta \sin\theta - \sin^2\theta)\,d\theta$$

$$= -\pi MP/4E\omega \qquad (79)$$

We now proceed to calculate $\Sigma(A_{2n-1} - A_{2n})$ of equation (76). When $\Delta\theta_{2n-1}$ and $\Delta\theta_{2n}$ are small in Fig. 4.9.

$$A_{2n-1} - A_{2n} \approx (P/\omega)\cdot(\sin\theta_{2n-1})\cdot(\Delta\theta_{2n-1} - \Delta\theta_{2n}) \qquad (80)$$

Combining equations (65) and (80), and taking the summation of $(A_{2n-1} - A_{2n})$ from 0 to $\pi/2$ by the same integrating technique, we have

$$\Sigma(A_{2n-1} - A_{2n}) \approx \int_0^{\pi/2} (MP/E\omega)\sin^2\theta\, d\theta = \pi MP/4E\omega \qquad (81)$$

From equations (76), (79), and (81), and use equation (73),

$$1 - 2\cos k\theta_1 + 2\cos k\theta_2 - \ldots + \cos\frac{k\pi}{2} = 0 \qquad (82)$$

Therefore, the odd harmonic components are zero.

It is to be noted, however, that the validity of equation (82) relies heavily on the assumption of negligibly small individual pulse width when compared with the period of the k^{th} harmonic. As a consequence, harmonics in the range of the switching frequencies of the bridge chopper can be expected to exist across points p and q of the chopper. These high-frequency harmonics, however, are easily attenuated to a negligible level by the small LC ac filter shown in Fig. 4.5. With these high-frequency harmonics removed from the properly-modulated pulses, a high-quality sine wave appears across the load, with the peak amplitude being defined by equation (72).

Computer Analysis of Harmonics

In the previous discussions concerning the fundamental component of load voltage and its harmonics, the approximate solutions for the algebraic sums of the cosine series on the right-hand sides of equations (71) and (82) are based on assumptions of negligible $\Delta\theta$'s. For a more accurate analysis, recurrence formulas of the successive θ's in Fig. 4.9 can be derived and solved by using a computer. These θ's can then be used to calculate more accurately the left-hand sides of equations (71) and (82).

The recurrence formulas for the θ's are obtained by solving equations (58) and (59) separately, where

$$E\theta_{2n-1} + M \cos \theta_{2n-1} = E\theta_{2n-2} + M \cos \theta_{2n-2} + \omega D \qquad (83)$$

$$E\theta_{2n} - M \cos \theta_{2n} = E\theta_{2n-1} - M \cos \theta_{2n-1} + \omega D \qquad (84)$$

For a specific inverter with given D, E, M, and ω, the successive θ's can be solved by starting with n = 1 and $\theta_o = 0$ in equation (83). The θ_1 obtained by the computer from equation (83) is then used in the right-hand side of equation (84) with n = 1 to solve for θ_2. This θ_2, in turn, is used to solve for θ_3 through equation (83) again, this time with n = 2. Thus, by alternating between equations (83) and (84) with successive n's, all the angles θ_1, θ_2, ... up to $\pi/2$ can be determined. These angles can be used subsequently to calculate the exact algebraic sums of the cosine series on the left-hand sides of equations (71) and (82). These exact results obtained from the computer analysis should provide a good indication as to how accurate the previous approximate solutions of the right-hand sides of equations (71) and (82) are. The computer program is given in Appendix E.

For input conditions E = 10 volts, M = 5 volts, ω = 377 rad/sec, and with D = 0.000615 for the volt-second capacity of the core T1 of Fig. 4.5, the computer analysis yields the following results, with the corresponding approximate results (obtained from the right-hand sides of equations (71) and (82)) listed inside the respective parentheses.

$$1 - 2 \cos \theta_1 + 2 \cos \theta_2 - .... + \cos \frac{\pi}{2} = 0.388753 \quad (0.392703)$$

$$1 - 2\cos 3\theta_1 + 2\cos 3\theta_2 - \ldots + \cos\frac{3\pi}{2} = 0.009235 \quad (\quad 0 \quad)$$

$$1 - 2\cos 5\theta_1 + 2\cos 5\theta_2 - \ldots + \cos\frac{5\pi}{2} = 0.017539 \quad (\quad 0 \quad)$$

As can be seen from the above data, good agreements exist between the computer results and the approximate analytical results. High degree of accuracy of the approximate solutions is therefore confirmed.

Self-Regulating Action

Equation (72) indicates that load-voltage regulation against the changes in E and V can be achieved without using a feedback closed-loop regulating system. If V and E are derived from the same dc source either directly or through a dc to dc converter, the ratio V/E can be kept constant despite possible fluctuations in the source voltage. Also, the very small power requirement of the sinusoidal signal $M \sin \omega t$ leaves little technical difficulty in keeping its amplitude M constant. With both (V/E) and M fixed, the self-regulating property of this inverter is evident from equation (72).

Test Circuit

A test circuit identical to that described in Fig. 4.5 has been built. The actual circuit components are listed in Table III. A 60-Hz sinusoidal signal is used for modulation purpose. The fundamental load voltage is found to be slightly

TABLE III

Actual Components for Fig. 4.5

C	:	5 μF
C1, C2	:	4.7 μF
C3, C4, C5, C6	:	0.04 μF
D1, D2, D3, D4	:	UTR 12
L	:	6 mH
N1, N2	:	100 turns, #28 AWG
N3, N4, N5, N6, N7, N8	:	35 turns, #28 AWG
Q1, Q2	:	T. I. 2N2906
Q3, Q4, Q5, Q6	:	G. E. 2N2909
R1, R2	:	2.7 kΩ
R3, R4	:	27 Ω
R5, R6, R7, R8	:	33 Ω
T1	:	52057-$\frac{1}{2}$A, Magnetics, Inc.
E, M, V	:	adjustable

less than the value defined by equation (72), due to the assumption of ideal lossless components in deriving that equation. For a constant ratio V/E = 3 and a constant sinusoidal signal M with a peak amplitude of 4.5 volts, the rms load voltage changes from 8.5 to 8.66 volts as voltage V varies from 20 to 40 volts and E varies simultaneously from 6.7 to 13.3 volts. Open-loop regulation within $\pm$ 1% is therefore accomplished for a $\pm$ 33% change of both V and E about their nominal values so long as their ratio remains constant. Figure 4.10 illustrates the per unit value n_a/n_o of the number of high-frequency cycles as a function of M/E, the theoretical curve being calculated from equation (69). Figure 4.11 shows oscillograms of the load voltage with and without filter. From the picture it can be seen that the high chopping frequency of the pulse-width modulator produces about 88 revolutions around the square-loop B-H characteristic of core T1 while tracing a single 60-Hz cycle. The frequency spectrum of filtered load voltage is shown in Fig. 4.12. The input-voltage conditions for Fig. 4.12 are E = 12 V, M = 9 V, and V = 37 V. Close to the theories, harmonics below the switching frequencies are inherently small, and those in the proximity of switching frequencies are effectively eliminated by the LC filter. The total harmonic content of Fig. 4.12 is about 1.9% of the fundamental component whose rms value is 17.5 volts for this particular set of input conditions.

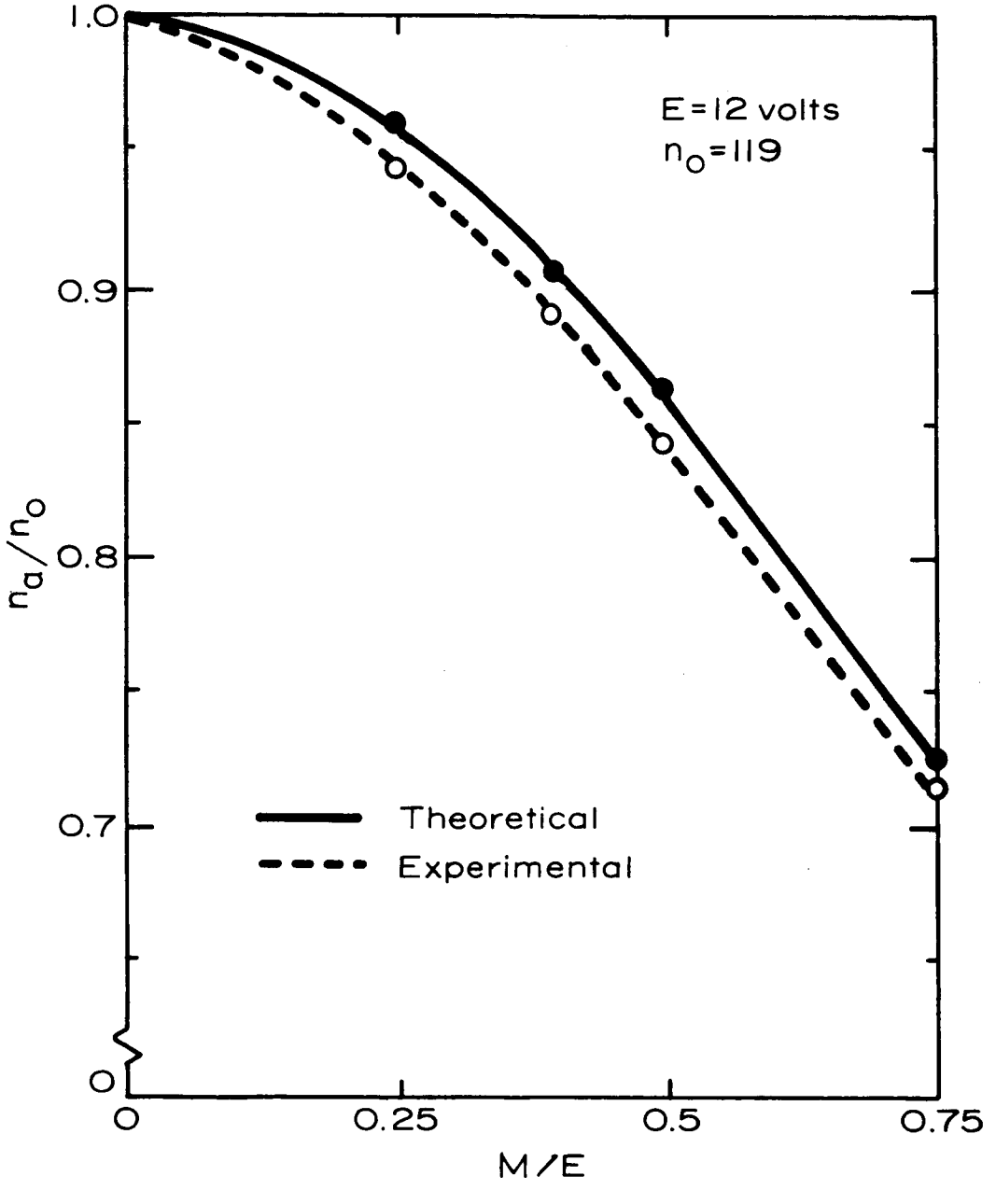

Fig. 4.10. Number of High-Frequency Cycles within a 60-Hz Low-Frequency Cycle.

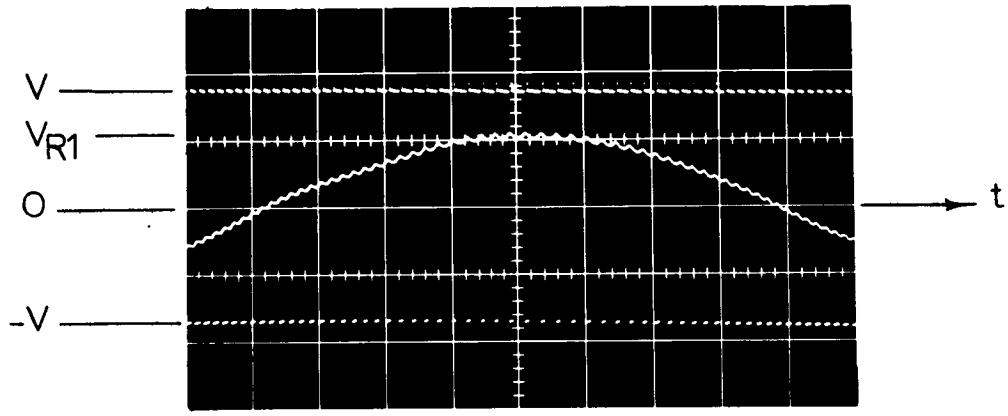

Fig. 4.11. A Half Cycle of Filtered and Unfiltered Load Voltage. The asymmetrical square-wave pulses are the unfiltered load voltage. Load voltage after filtering is the sine wave shown. The oscillogram is taken under the following conditions:

E = 12 volts, M = 9 volts, and

V = 37 volts.

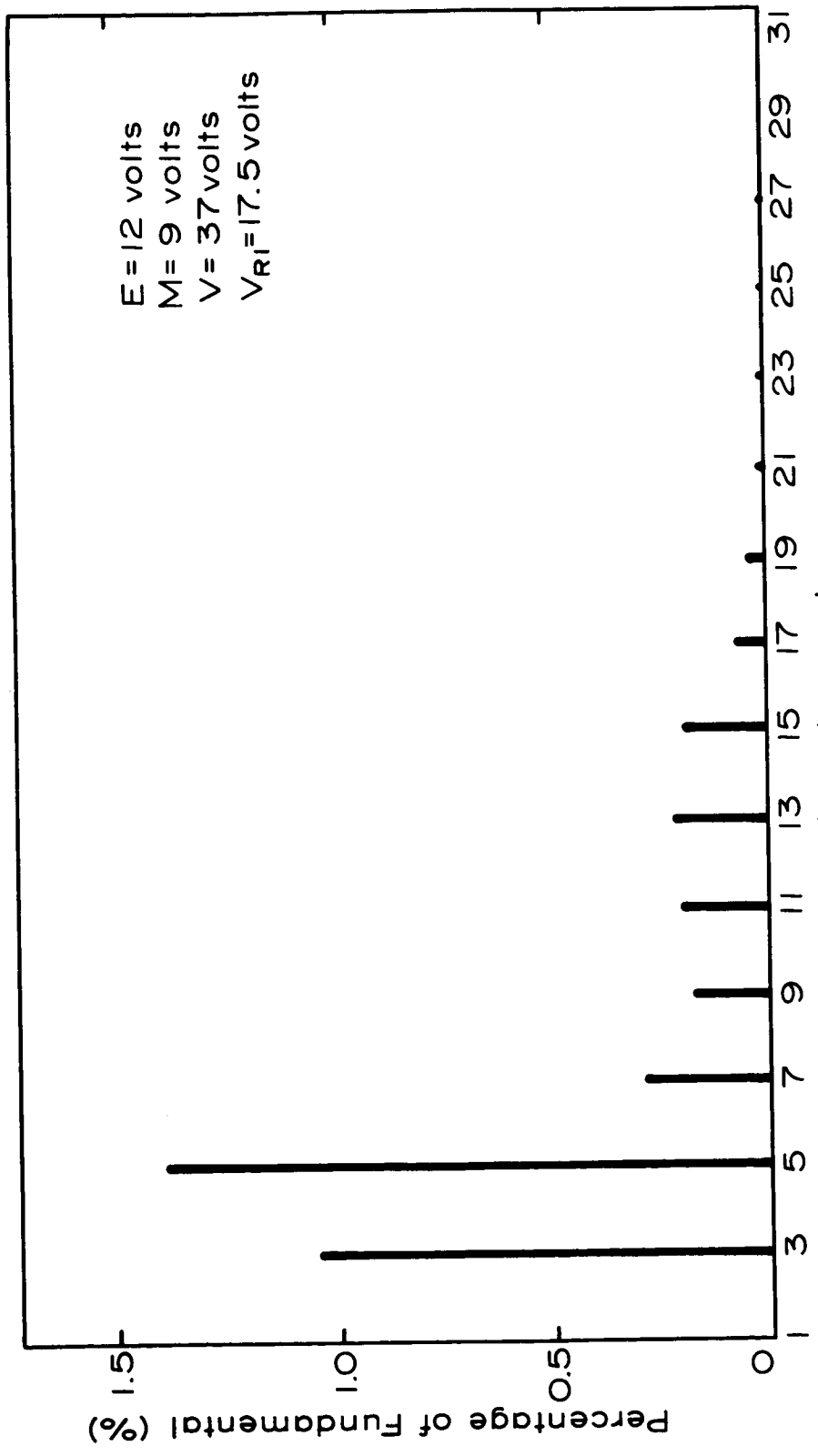

Fig. 4.12. Frequency Spectrum of the Filtered Load Voltage.

Future Circuit Improvement

In Fig. 4.5, two circuit improvements can be made to achieve the potentially high efficiency of this inverter:

(1) From Fig. 4.6(A), it can be seen that the amplitudes of the induced voltages across all the windings of Fig. 4.5, and therefore the base drives of the four transistors of the bridge chopper, are varied in a sinusoidal fashion. Since the resistors R5 to R8 must be designed to provide ample base drives for the respective conducting transistors when the induced voltages are at their minimum amplitudes, this base-drive scheme for the chopper transistors become very inefficient during the time when the induced voltages are high. In order for this situation to be remedied,nearly constant base drives must be provided for the four chopper transistors.

(2) The turn-off time (storage time plus fall time) of a switching transistor is normally longer than its turn-on time (rise time). As a result, the complete turn-on of chopper transistor Q4 and Q5 occurs before the complete turn-off of Q3 and Q6, and vice versa. Therefore, the two transistors on the same side of the bridge which are designed to pass currents during the two different half cycles (Q3 and Q4, or Q5 and Q6), conduct simultaneously for the time

differential between their turn-on and turn-off times. When this happens, a near short circuit with impedance equivalent to the combined impedances of the two conducting transistors is placed across the dc source V. This reduces considerably the efficiency of the inverter. To limit this loss, proper circuitries must be provided to delay the turn-on and to speed up the turn-off of the respective transistors.

With nearly constant base drives for the power transistors Q3 to Q6, and with negligible short-circuit current in the bridge chopper, the potentially high efficiency of this inverter can then be realized in practical power applications.

Conclusion

In addition to providing a mathematical foundation for the technique of pulse-width modulation as applied to the dc to sine wave inverter, this chapter describes a static inverter in which high-frequency chopping with a sine-wave modulation is accomplished through a simple switching control consisting of two transistors and a square-loop core. Since all transistors are operated in the switching mode, the inverter efficiency should be high if the aforementioned two improvements are made. Substantial savings in the size and weight of the inverter are achieved as it requires no power transformer and no low-frequency filter components.

Due to the inherent self-regulating action of the inverter, nearly constant load voltage is maintained against input-voltage change without requiring additional regulating elements.

The primary objective of this chapter has been to illustrate the basic principle of the pulse-width modulation. In this regard the test inverter circuit handles only a small amount of power at a low voltage level and is not designed to meet any application-oriented requirement. Features such as closed-loop regulation or short-circuit protection are not attempted, although such requirements can be realized with simple circuit modifications. With the recent availability of high-voltage fast-switching power transistors, the inverter should be able to supply 115-volt 400-hertz sinusoidal voltage for aerospace applications. Additionally, it is to be noted that the frequency $\omega/2\pi$ of the sinusoidal modulating signal $M \sin \omega t$ can be varied over a wide range, which suggests other possible applications for this inverter such as audio amplifications and speed control of ac motors.

CHAPTER V

CONCLUSION

Space vehicles, launched by rockets and injected into earth satellite orbits, require light-weight, self-contained power sources to energize radio transmitters and receivers, scientific instruments, attitude control devices, and other apparatus. Thus far these sources have been characterized by their low dc voltage outputs. Also, the available voltage levels of these sources vary with the environmental conditions of the sources such as light intensity and temperature. Due to the requirements of spacecraft electrical loads for power in various forms and at voltage levels that are quite different from these low dc source voltages, certain power-conditioning processes are required to provide the necessary compatibility between the sources and the loads. Because of the complete lack of maintenance aboard the space vehicles, only solid-state and static magnetic components are normally used in these power-conditioning systems.

Depending on different input conditions and output requirements, three of the more important functions performed by these power-conditioning systems between the sources and the loads are:

(1) To perform the step-up of direct source voltages from a fraction of a volt to alternating or direct voltages at higher levels. The tunnel diodes, with their inherent low-voltage negative-resistance characteristics, are particularly suitable for applications involving extremely low voltage conditions.

(2) To maintain essentially constant load voltages despite variations in the source voltages and the load demands. Transistors and SCR's are used rather extensively in these systems.

(3) To transform from variable direct source voltages to sinusoidal ac voltages of constant amplitudes at specified frequencies.

The research programs described in this dissertation are divided into three major parts, with each part dealing with one of the three aforementioned important functions. After an introductory chapter which defines the scope of work, the three research topics are:

(1) In Chapter II, the analysis of the Marzolf tunnel diode inverter is performed with emphases on functional subtleties such as the steps, spikes, and curvatures associated with the induced-voltage waveform. The performance and the critical line and load conditions of the normal square-wave oscillations of this inverter are analyzed. Spikes and curvatures of the induced voltages are found to be related to the nonlinear tunnel diode charac-

teristics and the fact that the mmf of the saturated core and/or the source inductance cannot change instantaneously. Equations are derived to predict the amplitudes of the spikes and curvatures under different line and load conditions. The zero-voltage step intervals of the induced-voltage waveform are found to be caused by the inadvertent existence of some source inductance, and are calculated theoretically. The effect of source inductance increases with the current ratings of the tunnel diodes. Since the complete absence of source inductances from the available practical sources is impossible, steps of zero voltage are inevitable in high-current Marzolf tunnel diode inverters. As the presence of these unwanted steps drastically reduces the already-low inverter efficiency, one cannot but cast a dim prospect on the future of this type of high-current tunnel diode inverters.

(2) Chapter III describes an efficient, physically-simple, dc to dc regulated converter using the basic principle of inductive-energy storage and release. Regulation of the converter is maintained by controlling both the on time and the off time of the main power switching transistor. The inversion frequency range of this converter is much smaller than other variable-frequency converters with either a constant on time or a constant off time. Consequently, less difficulties are encountered in making

the proper compromises among the various performance characteristics involving size, weight, efficiency, stability, and ripple, resulting in the good overall performance of this converter. Measured efficiencies over ninety percent were obtained for the test circuit with an input-voltage range of 12 to 28 volts and an ouput-load range of 4 to 20 watts. The physical simplicity of this converter is also attractive from a reliability and cost viewpoint. Due to the wide range of control provided by the voltage-to-duty-cycle encoder described in Chapter III, the converter configuration should be particularly suited for operating under widely changing line and load conditions.

(3) Discussed in Chapter IV is a light, efficient, self-regulating dc to sine-wave inverter using techniques of high-frequency pulse-width modulation. The switching frequency of the inverter is very high compared to the frequency of the sinusoidal output voltage. While a similar technique has been employed intuitively in other recently-developed dc to sine-wave inverter circuits to reduce the harmonic amplitudes of the fundamental sinusoidal output voltages, no rigorous mathematical proof of the fact has been demonstrated. Chapter IV provides the needed mathematical foundation of this technique by proving analytically the small

amplitudes associated with the harmonics of the sinusoidal output voltages. In addition to the analytical studies, the inverter described in Chapter IV is also suited for practical dc to sine-wave inversion. The requirements of low-frequency output transformer and low-frequency filter components are eliminated. Furthermore, an essentially constant sinusoidal output voltage of the inverter is maintained in an open-loop fashion, thus adding to its versatility and its potential for practical applications. With the sure prospect of faster and better semiconductor switches in the future, efficient and light-weight dc to sine-wave power inverters using the technique of pulse-width modulation are to be expected.

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APPENDICES

APPENDIX A

EFFECT OF SOURCE INDUCTANCE WHEN THE TWO DIODES ARE OPERATING ON TWO DIFFERENT VOLTAGE SEGMENTS

Assume the tunnel diodes used in the inverter has an idealized N-characteristic such as that shown in Fig. 2.7(B), where current in diode #1 is increasing along the low-voltage segment and that of diode #2 is decreasing along the high-voltage segment of their respective i-v characteristics. Then,

$$v_1 = i_1 r \tag{A.1}$$

$$v_2 = V + i_2 r \tag{A.2}$$

where r and V are defined in Fig. 2.7(B).

For simplicity, assume the inverter is operating at no load. Thus,

$$N\dot{\phi} = L_w(\dot{i}_1 - \dot{i}_2) \tag{A.3}$$

where $L_w = N^2K$ is the winding inductance of the inverter when the core is saturated. Substitute equations (A.1), (A.2), and (A.3) into equations (1) and (2) and perform their sum and their difference,

$$2L_s(\dot{i}_1 + \dot{i}_2) + (r + R + 2R_s)(i_1 + i_2) = 2E_i - V \qquad (A.4)$$

$$2L_w(\dot{i}_1 - \dot{i}_2) + (r + R)(i_1 - i_2) = V/2 \qquad (A.5)$$

Let P and P′ be the initial difference and the initial sum of the two currents respectively, then, solve equations (A.4) and (A.5) for $(i_1 + i_2)$ and $(i_1 - i_2)$,

$$i_1 + i_2 = \frac{2E_i - V}{r + R + 2R_s} + (P' - \frac{2E_i - V}{r + R + 2R_s}) \exp(- \frac{r + R + 2R_s}{2L_s})_t \qquad (A.6)$$

$$i_1 - i_2 = \frac{V}{r + R} + (P - \frac{V}{r + R}) \exp(- \frac{r + R}{2L_w})_t \qquad (A.7)$$

From equations (A.6) and (A.7),

$$i_1 = \tfrac{1}{2}\left[(\frac{2E_i - V}{r + R + 2R_s} + \frac{V}{r + R}) + (P' - \frac{2E_i - V}{r + R + 2R_s}) \exp(- \frac{r + R + 2R_s}{2L_s})_t - (\frac{V}{r + R} - P) \exp(- \frac{r + R}{2L_w})_t\right] \qquad (A.8)$$

$$i_2 = \tfrac{1}{2}\left[(\frac{2E_i - V}{r + R + 2R_s} + \frac{V}{r + R}) + (P' - \frac{2E_i - V}{r + R + 2R_s}) \exp(- \frac{r + R + 2R_s}{2L_s})_t - (\frac{V}{r + R} - P) \exp(- \frac{r + R}{2L_w})_t\right] \qquad (A.9)$$

For a typical inverter design, the winding inductance L_w is much greater than the source inductance L_s. The expotential factors involving L_s in equations (A.8) and (A.9) are therefore decreasing much faster than those involving L_w. Also, $(\frac{V}{r + R} - P)$ is normally an order of magnitude greater than $(P' - \frac{2E_i - V}{r + R + 2R_s})$. Consequently, if very accurate analysis is not required in favor of simplicity, the effect of source inductance is negligible during the operations of the inverter when the two diodes are migrating on two different positive-resistance segments of their respective characteristics.

APPENDIX B

EFFECT OF SOURCE INDUCTANCE AS RELATED TO THE CURRENT RATINGS OF THE TUNNEL DIODES USED IN THE MARZOLF INVERTERS

While the current rating of tunnel diodes range from milliamperes to hundreds of amperes, the peak voltages and the valley voltages are relatively unchanged for tunnel diodes made of the same material. The following specifications are assumed for two tunnel-diode pairs,

Diode Pair A: $V_p = 60$ mV, $V_h = 400$ mV, $I_p = 20$ mA,
$I_v = 2$ mA, and $r = V_p/I_p = 3$ ohms

Diode Pair B: $V_p = 60$ mV, $V_h = 400$ mV, $I_p = 100$ A,
$I_v = 10$ A, and $r = V_p/I_p = 6 \times 10^{-4}$ ohms

Additionally, assume the tunnel diode inverter of Fig. 2.2 has the following associated parameters:

$E_i = 225$ mV, $R = 10^{-4}$ ohms, $R_s = 10^{-4}$ ohms, and $L_s = 0.75$ μH

For the inverter employing diode pair A, the step interval can be calculated from equation (36), assuming both diodes are operating on the low-voltage segment during the step interval. Then,

$$T_{step} = \frac{1.5 \times 10^{-6}}{3.0003} \ln \frac{394}{374} = 0.025 \times 10^{-6} \text{ sec} = 0.025 \ \mu\text{sec}$$

On the other hand, if diode pair B is used in the inverter,

$$T_{step} = \frac{1.5 \times 10^{-6}}{0.9 \times 10^{-6}} \ln \frac{394}{308} = 0.407 \times 10^{-6} \text{ sec} = 407 \ \mu\text{sec}$$

Therefore, with identical source impedance and circuit resistance, the step interval increases from 0.025 microseconds for the inverter with small-current tunnel diodes to 407 microseconds for that with high-current diodes - an increase of approximately 16200 times. Since the ratio of the peak currents for the diodes is 5000, the effect of source inductance increases in the same order with the current ratings of the tunnel diodes.

APPENDIX C

RINGING PHENOMENON

During the interval t_{off}'', diode D1 is reverse-biased, which effectively isolates the input and the output portions of the converter. The part of the circuit to the left of D1 in Fig. 3.4 resembles a series RLC circuit with L the inductance of the energy-storage reactor, C the junction capacitance associated with the power transistor Q1 (primarily the capacitance of the base-collector junction as it accounts for most of the depletion layer capacitance of the transistor),[30] and R the combined effective resistance of winding N7, the parallel combination of R5-C4, winding N1, and the input source supplying E_i. The voltage across the effective emitter-collector capacitance of transistor Q1 has an initial magnitude at the beginning of t_{off}'' that is slightly less than the sum of the output voltage E_o plus the forward drop across D1. Consequently, the voltage across N1 undergoes damped sinusoidal oscillations with the energy initially stored in the junction capacitances of Q1 acting as the primary sources. During these oscillations which take place in the interval t_{off}'', the control voltage e_c continues to move the flux of core T2 toward negative saturation. Depending on the magnitude of e_c, the oscillatory voltage across N1 may or may not have decayed to zero before the end of t_{off}''. The latter condition is the case for Fig. 3.6(B).

Since the winding N7 is part of the series RLC circuit, this ringing during t_{off}'' has some significant effects on the

operation of the asymmetrical multivibrator. Depending on whether energy is being transferred from L to C or from C to L, the ringing current flows into or out of the dotted end of N7, and the component of the ringing voltage that is across N7 causes the voltage at the dotted end of all windings on T2 to be more positive or more negative. Notice in Fig. 3.4 that the magnetizing current for core T2 during t_{off}'' is flowing out of the dotted end of N4, and the voltage at the dotted end is negative. Consequently, during the time in t_{off}'' when energy is being transferred from L to C, the ringing current of N7 appears as load current to winding N4, and the ringing voltage across N7 tends to reduce the voltage in the base circuit of transistor Q3. To overcome this increased load current, voltage e_c must supply more current through N4 while simultaneously there is less base drive for Q3. This presents no problem as long as e_c is sufficiently large, as it is for the case shown in Fig. 3.6(B). However, since e_c diminishes with the output load, there is a certain reduced load at which e_c will no longer be sufficient to provide ample base drive for Q3 to conduct the required current. When this happens, core T2 begins to operate on minor B-H loops during a portion of t_{off}''. This is discussed in detail in Appendix D.

APPENDIX D

MINOR-LOOP OPERATION

An oscillogram of the voltage across and the current through the energy-storage reactor under the minor-loop operation when e_c is quite low is shown in Fig. D.1. For this particular condition of line and load there are two cycles of minor-loop operation before the flux of core T2 completes a revolution around its major B-H loop. The longest on time in Fig. D.1 corresponds to a flux excursion from negative saturation to positive saturation of core T2, while the two successively shorter on times correspond to flux excursions from intermediate flux levels to positive saturation. At the end of each of these on-time intervals, the flux of core T2 is at positive saturation.

To examine in detail the operation of the converter under the condition of minor-loop operation, the flux of core T2 is assumed to be at negative saturation at the beginning of t_{on}. At the same instant, the flux of core T1 is at the residual level B_r. The conduction of transistor Q2 turns on the power transistor Q1. The flux in each of the two cores moves upward until T2 reaches positive saturation at which time Q2 blocks and Q3 conducts, removing base drive from Q1. Neglecting the storage time of Q1, the turning on of Q3 marks the beginning of t_{off}' and the downward flux movement in each core. The flux of core T1 then reaches B_r at the end of t_{off}',

at which time t_{off}'' begins and the ringing of the RLC circuit starts with the transfer of energy from C to L as described previously. Current flows out of the dotted end of both N4 and N7, and the flux of T2 continues to move toward negative saturation. However, after the first half cycle of ringing, the energy transfer reverses, sending current now from L to C. At this time the flux of core T2 is somewhere between the two saturation levels at a distance $\Delta\phi$ from positive saturation when suddenly e_c becomes too small to sustain the required current, as explained previously. Flux of each core now starts to move upward again until T2 saturates at positive saturation. When T2 saturates, Q2 blocks, Q3 conducts, and Q1 turns off. Since $\Delta\phi$ of core T2 is smaller than the flux excursion between the two saturation levels, this t_{on} conduction time for transistors Q1 and Q2 is less than the preceding t_{on}. This shorter conduction time results in a smaller upward flux excursion of core T1. Since the rate at which the flux of T1 moves toward B_r following the conduction of Q3 is constant and is equal to $(E_o - E_i)/N_1$, the smaller upward flux excursion in core T1 causes a shorter t_{off}', which in turn causes the next $\Delta\phi$ to be smaller before the magnetizing current of T2 is lost again due to the ringing effects reflected from N7 to N4. The same process repeats itself with successively smaller $\Delta\phi$'s until the core effectively hangs at positive saturation of T2. When this happens, the induced voltage across N3 following the sudden loss of magnetizing current in N4 due to the first transfer of energy from L to C is now too small to provide enough base drive

for Q2, therefore, Q2 stays blocking and Q1 remains off. The energy transfer from C to L follows, with current flowing out of the dotted end of N7. The combined effects of this ringing and the voltage e_c then initiates the downward flux movement of core T2. At the end of this particular half cycle of ringing, a total of three half cycles of oscillation has occurred, with dissipation of energy in each of the three half cycles. By this time the effect of the ringing is no longer strong enough to cause a sudden loss of magnetizing current for core T2 during the successive transfer of energy from L to C. A cycle of long t_{off}" therefore occurs, and flux of core T2 reaches negative saturation, at which point a new series of minor-loop operations is ready to start again.

The minor-loop operation is difficult to predict from a design point of view. Nevertheless, it happens only at light load, and it is not detrimental to the proper functioning of the converter since output regulation is still maintained by the feedback loop. It should be noted also, that if deemed desirable, the effects of the ringing can be eliminated at the expense of efficiency. This can be accomplished either by placing a resistive element across Q1 to dissipate some of the initial energy stored in the junction capacitances or by inserting a diode in the base circuit of the power transistor Q1 to block the ringing current which would flow through N7 from L to C. With the elimination of the effects of ringing, the minor-loop operation described here does not occur.

Due to the somewhat random nature of the minor-loop operations, some low-frequency ripples do occur in a random fashion at certain line and load conditions. Their amplitudes, however, are very small, a maximum of 40 millivolts being observed for the test circuit.

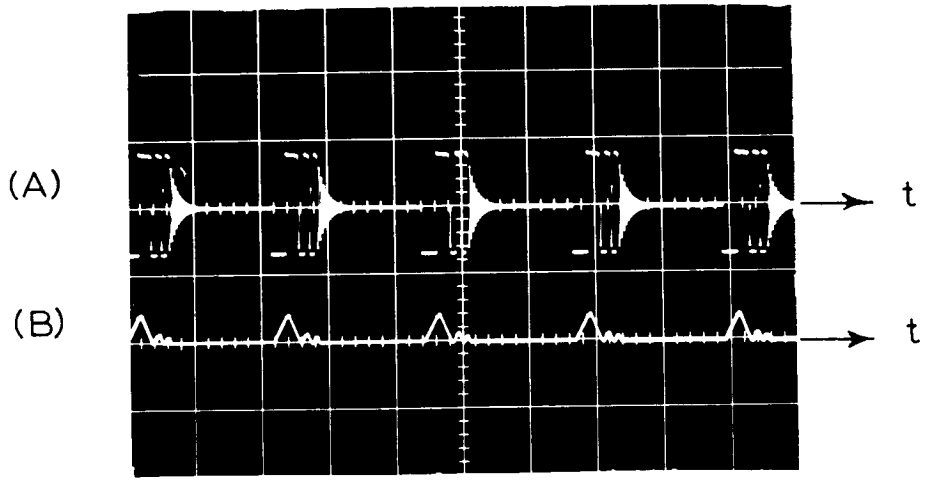

Fig. D.1. Voltage and Current of Energy-Storage Reactor at Minor-Loop Operation.

(A) Induced Voltage at E_i = 14 V, P_o = 0.5 W

(B) Winding Current at E_i = 14 V, P_o = 0.5 W

APPENDIX E

COMPUTER PROGRAM FOR HARMONIC ANALYSIS

```
BEGIN
REAL E,M,LL,W,D,KK,GG,A,R,T,U,Q,V,Y;
INTEGER N, S, H;
ARRAY  B[0:400], A[0:400], P[0:400], X[0:400] ;
READ E,M,W,D,S ;
     X[0] := 0 ;
     P[0] := 0 ;
     A[0] := 0 ;
     B[0] := 0 ;
FOR N := 1 STEP 1 UNTIL S DO
BEGIN
WRITE N ;
SPACE(120) ;
     LL := E*B[N-1] + ((-1)**(N-1))*(M*COS(B[N-1])) + W*D ;
     B[N] :=B[N-1] ;
GR :
     GG := E*B[N] - ((-1)**N)*(M*COS(B[N])) ;
     KK := LL - GG ;
IF KK GRT 0.00025 THEN GO TO YU ELSO GO TO LEE ;
YU:
     B[N] := B[N] + 0.0001 ;
GO TO GR ;
LEE:
FIX(B[N], 1, 5) ;
SPACE(120) ;
     H := N ;
IF B[N]>1.570798 THEN GO TO HU ;
END ;
HU:
FOR N := 1 STEP 1 UNTIL H DO
BEGIN
     FIX(N, 3, 0) ;
SPACE(6) ;
FIX(B[N], 1, 6) ;
SPACE(6) ;
     R := ((-1)**N)*(COS(B[N])) ;
     A[N] := R + A[N-1] ;
     Q := 1 + 2*A[N] ;
     FIX(Q, 1, 6) ;
SPACE(6) ;
     T := (COS(3*B[N]))*((-1)**N) ;
     P[N] := T + P[N-1] ;
     U := 1 + 2*P[N] ;
     FIX(U, 1, 6) ;
SPACE(6) ;
     V := (COS(5*B[N]))*((-1)**N) ;
```

```
        X[N] := V + X[N-1] ;
        Y := 1 + 2*X[N] ;
        FIX(Y, 1, 6) ;
SPACE(6)
SPACE(120) ;
END ;
END ;
```

BIOGRAPHY

Name: Yuan Yu

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Place of Birth: Foncheng, China

Universities Attended:	Dates	Degree	Date of Degree
National Taiwan University	1955-1959	BSEE	June 1959
Washington State University	Summer 1961		
Duke University	1961-Present		

Major: Electrical Engineering

Minor: Physics and Mathematics

Publications:

1. _____, with W. E. Hammond, T. G. Wilson, I. M. H. Bábaá, and E. T. Moore, "A D-C to D-C Converter Using Two Synchronized Complementary Converters," Supplement to IEEE Transactions on Aerospace, vol. AS-3, no. 2, June 1965, pp. 201-209.

2. _____, with I. M. H. Bábaá, E. T. Moore, T. G. Wilson, and W. E. Hammond, "Dc-to-Dc Converter Using Inductive-Energy Storage for Voltage Transformation and Regulation," IEEE Transactions on Magnetics, vol. MAG-2, no. 1, March 1966, pp. 18-25.

3. _____, with Donald L. Hester and Thomas G. Wilson, "Analytic Model for Describing the Operation of the Marzolf Tunnel Diode Inverter," IEEE Transactions on Magnetics, vol. MAG-2, no. 3, September 1966, pp. 632-638.

4. _____, with T. G. Wilson, I. M. H. Babaa, and E. T. Moore, "Dc to Dc Converter Controlled by a Magnetically-Coupled Multivibrator with Asymmetrical Output," Proceedings of the National Electronics Conference, vol. 22, October 1966, pp. 265-270.

Honorary Societies: Sigma Xi

Positions Held:

September 1961 - June 1964	Part-time Teaching Assistant, Electrical Engineering Department, Duke University, Durham, North Carolina
June 1964 - Date	Full-time Research Assistant, Electrical Engineering Department, Duke University, Durham, North Carolina